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Advancing the Standard

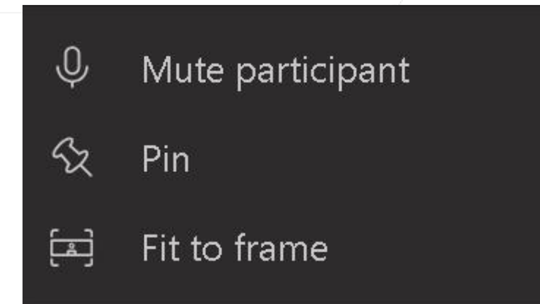
April, 2024

LAB

Simulation of Projection Lithography

Pre-Cursor

- IMPORTANT NOTICE: Please note that this session will be recorded. By joining these webinar sessions, you automatically consent to such recordings.
  - Q&A will not be recorded



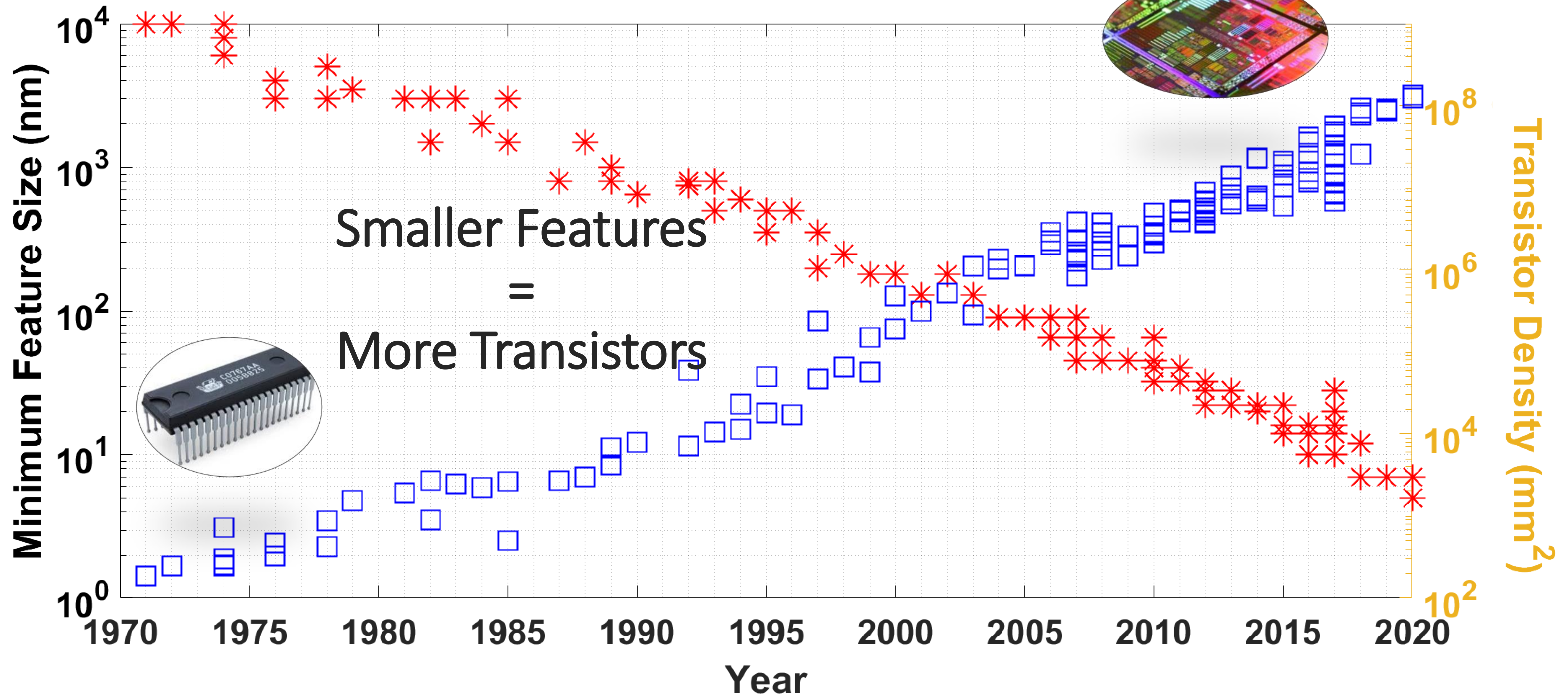
- MS Teams essentials (**App Users**):
  - Right click on image, use „Pin“ to enlarge

- This webinar is an overview / introduction to projection lithography simulation
  - It picks out essential ingredients, focus on applications in the field.
  - In case you want / need more depth -> Contact support@genisys-gmbh.com

Outline

- Projection Lithography
- 3D Exposure Simulation
- Application Cases
- Summary

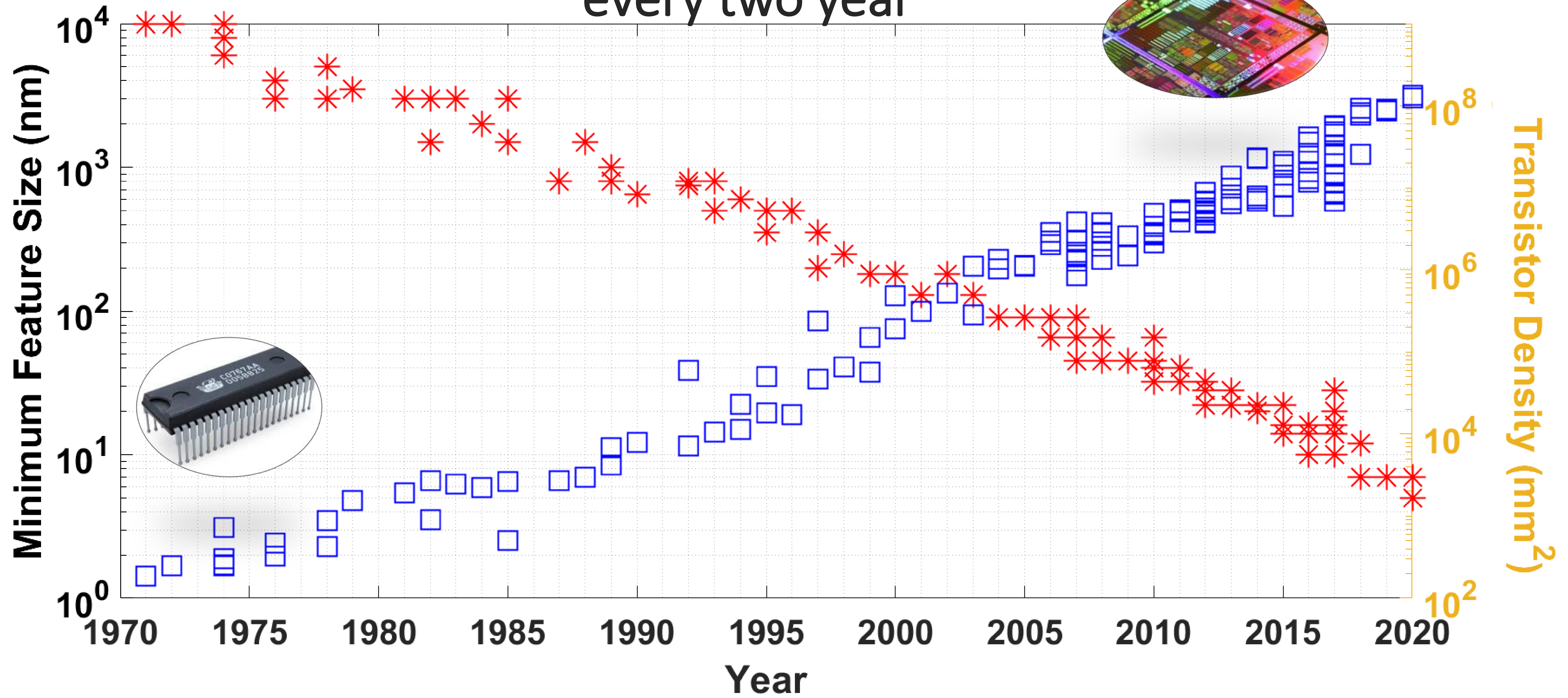
Miniaturization Trend



Data from: https://en.wikipedia.org/wiki/Transistor_count

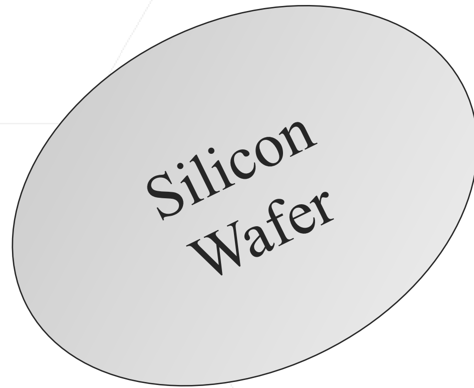
Number of transistor doubles every two year

Moore´s Law

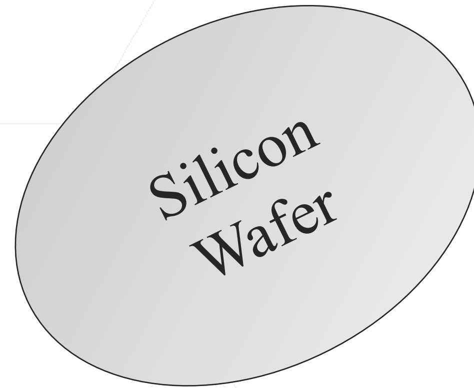


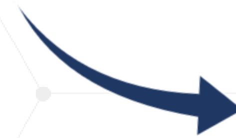
Data from: https://en.wikipedia.org/wiki/Transistor_count

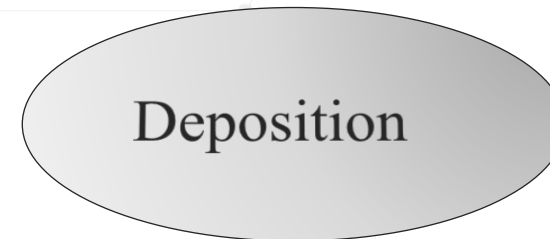
Chip Production Process



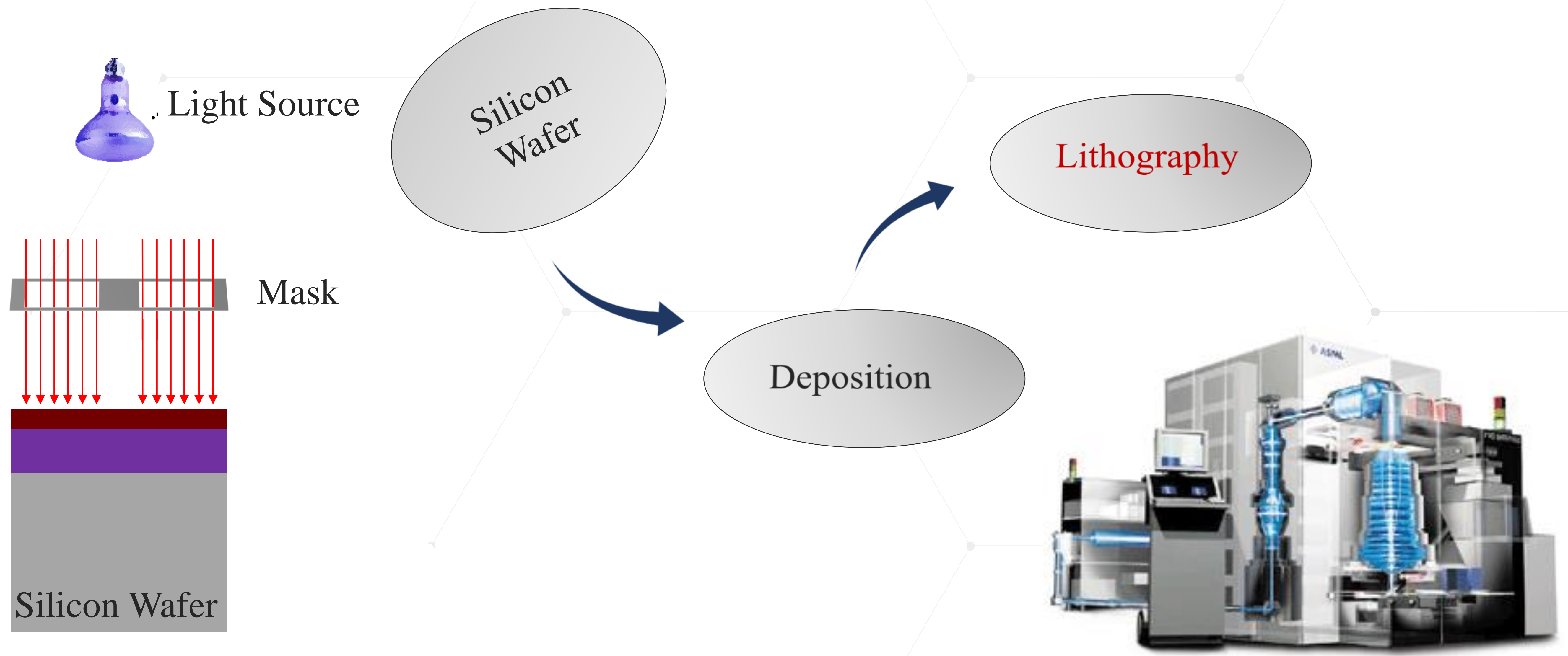
Chip Production Process



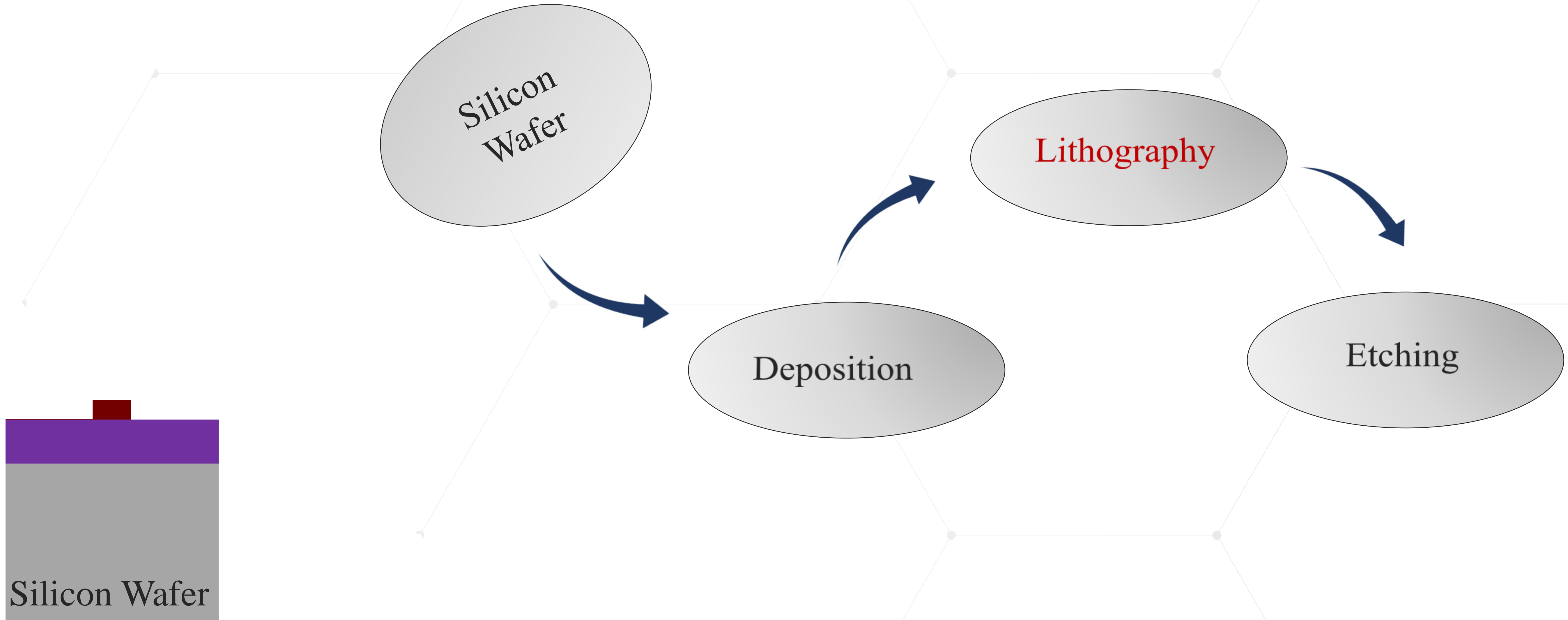




Chip Production Process



Chip Production Process



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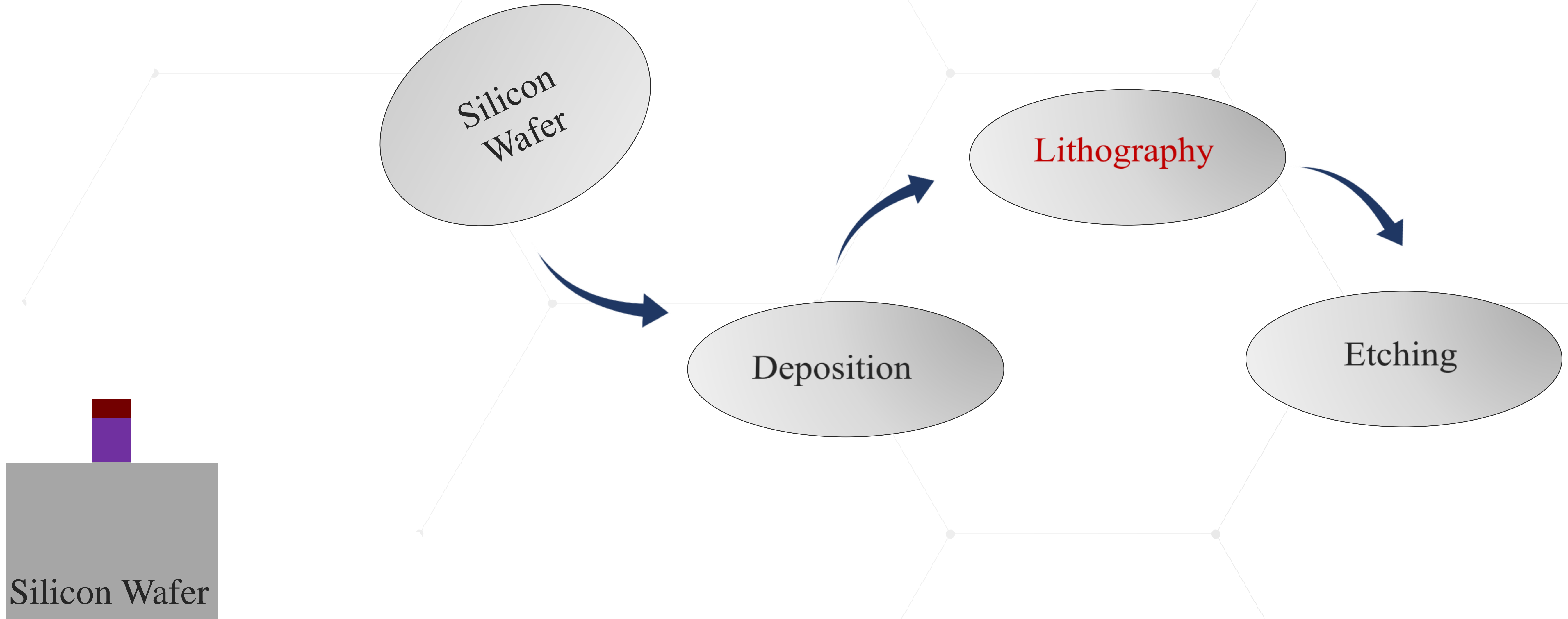
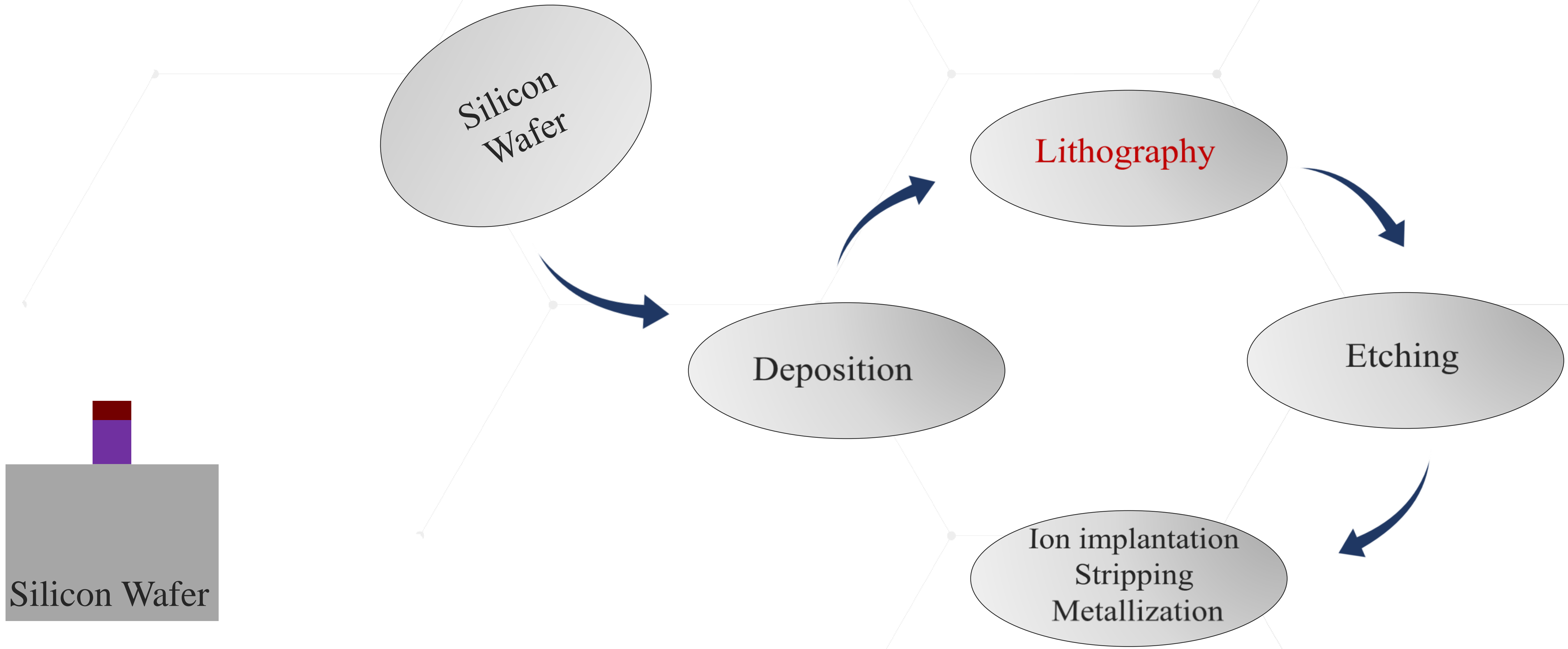
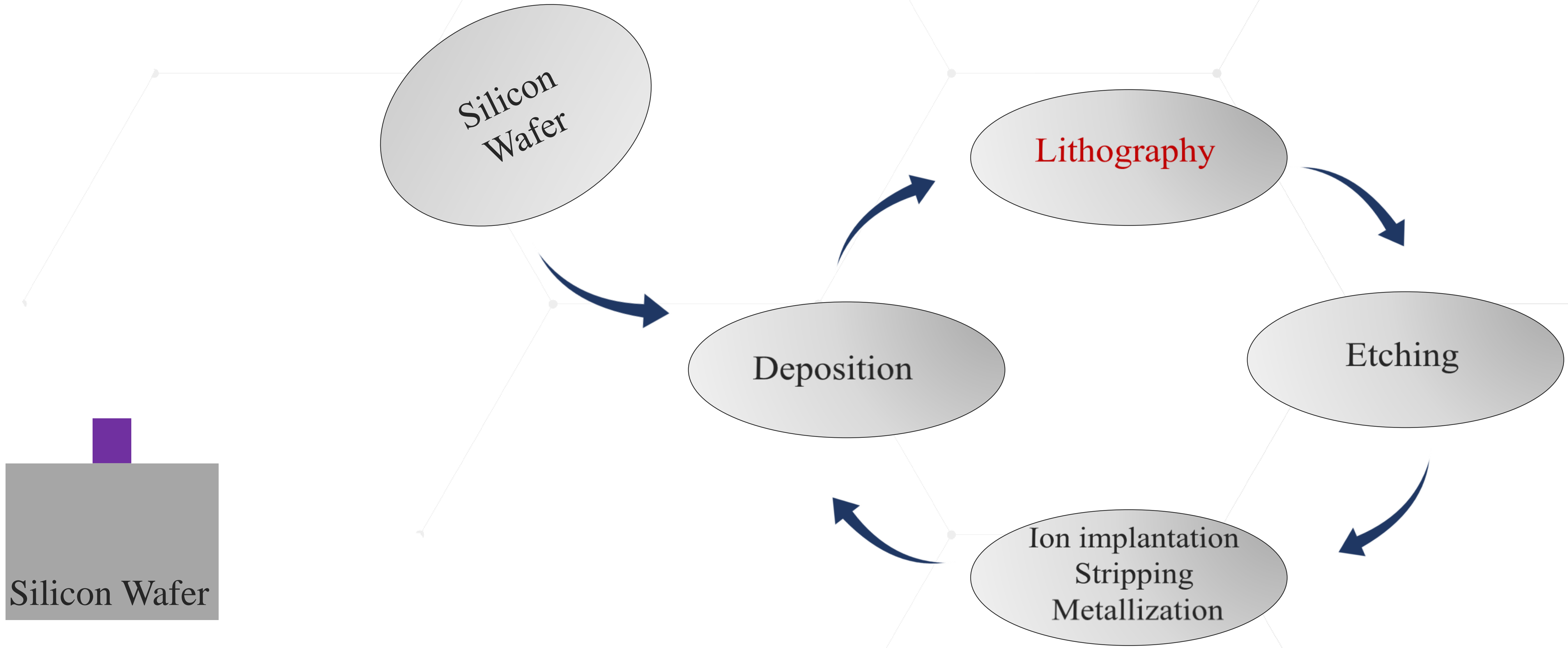
Chip Production Process



Chip Production Process



Chip Production Process



Chip Production Process

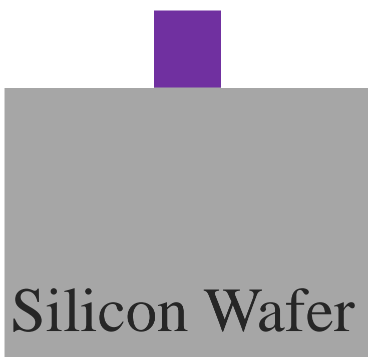
Silicon Wafer

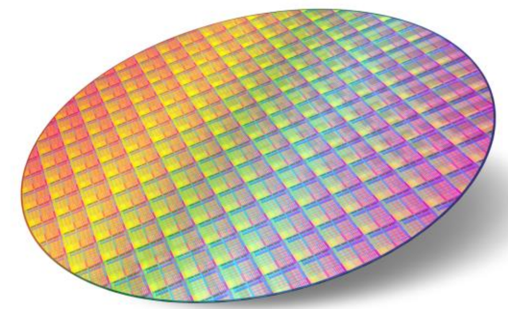
Lithography

Deposition

Etching

Ion implantation
Stripping
Metallization





Lithography is limiting miniaturization

Lithography Scaling

Lithography scaling

6.1 µm (Nodes)
Lamp
KrF
ArF
Plasma
3 µm
2 µm
1.5 µm
1 µm
0.8 µm
0.7 µm
0.5 µm
0.35 µm
0.25 µm
180 nm
130 nm
90 nm
65 nm
45 nm
32 nm
22 nm
15 nm
400 – 440 nm
436 nm
356 nm
248 nm
193 nm
193 nm wet
13.5 nm
EUV
Microns
10
1
0.1
0.01
1970 1975 1980 1985 1990 1995 2000 2005 2010 2015 2020
Year

Resolution Enhancement Techniques enabled Moors law

The Rayleigh Resolution Equation

$$R = k1 \frac{\lambda}{NA}$$

R = the smallest “half pitch” that can be printed

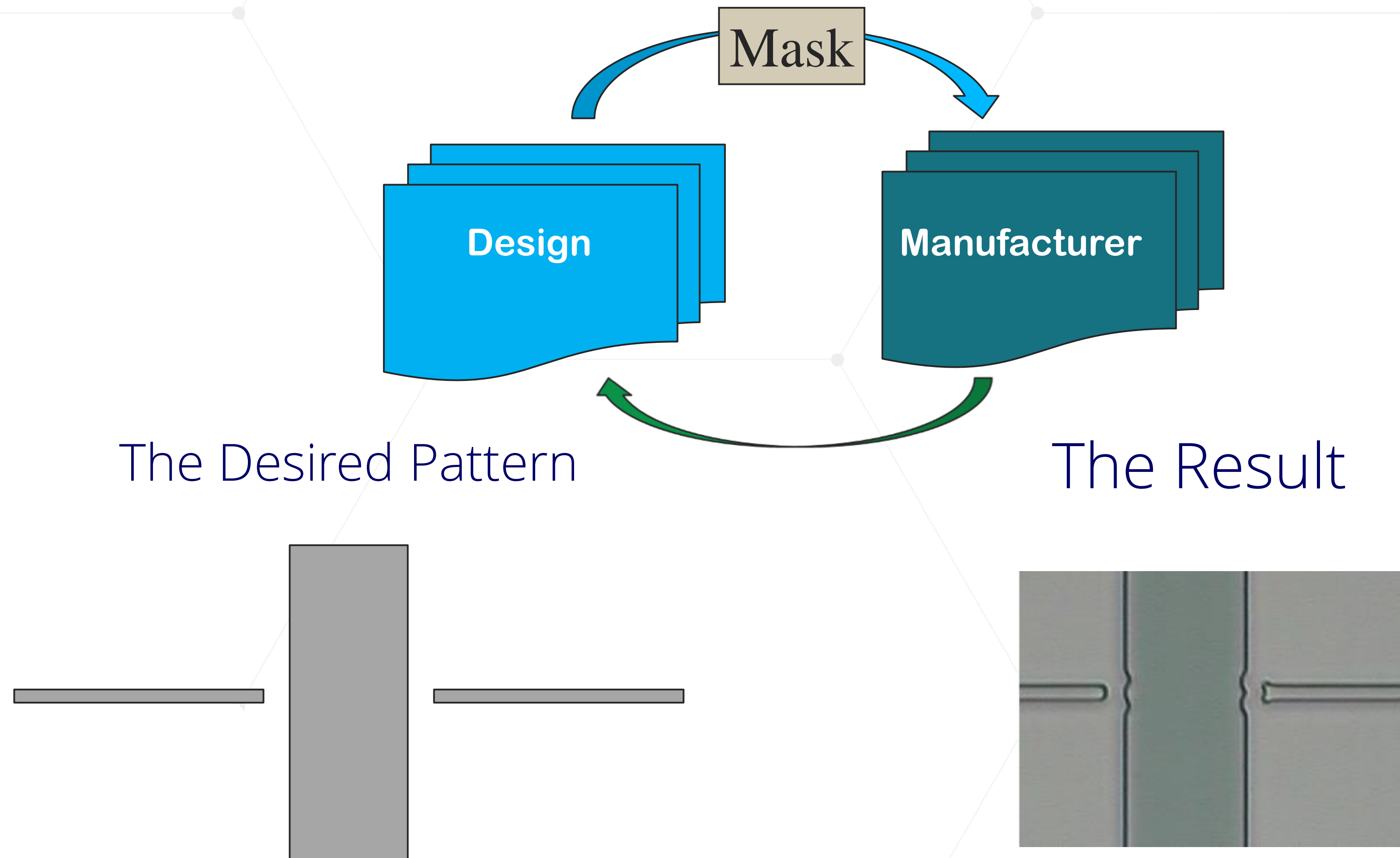
Improving resolution:

- Lower wavelength
- Increase Numerical Aperture
- Lower k1 factor

k1 – factor which includes photoresist improvements and application of **Resolution Enhancement Technologies**

Why Lithography Simulation?

- Simulation becomes a must for process optimization ahead of fabrication.



Experiment is time consuming and expensive → Simulation

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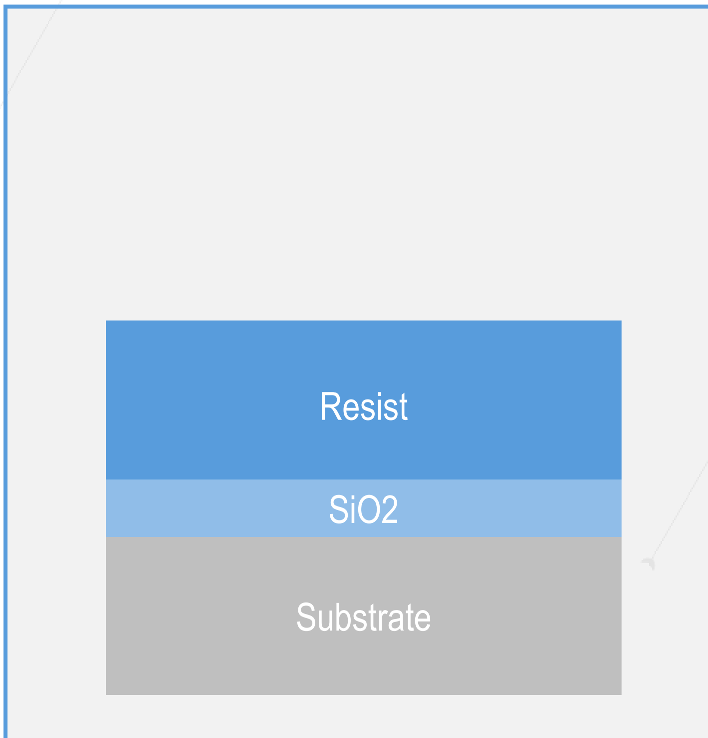
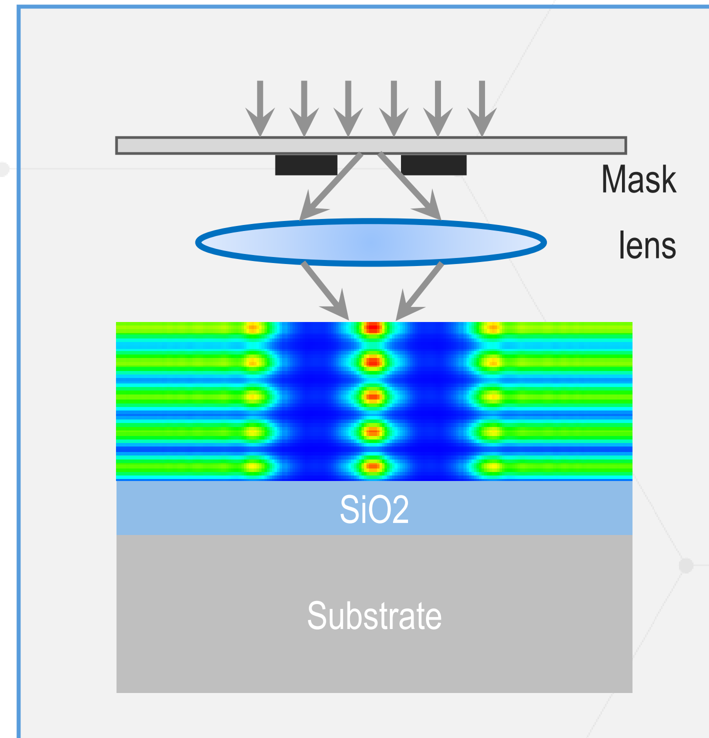
Lithography Simulation

- Projection simulation: optical exposure and resist development.

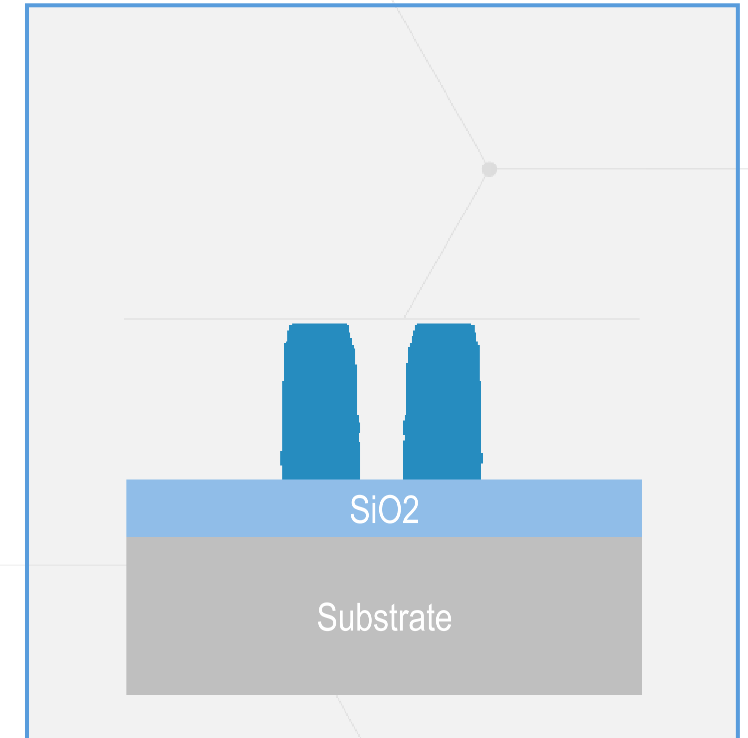
Wafer preparation



Optical exposure

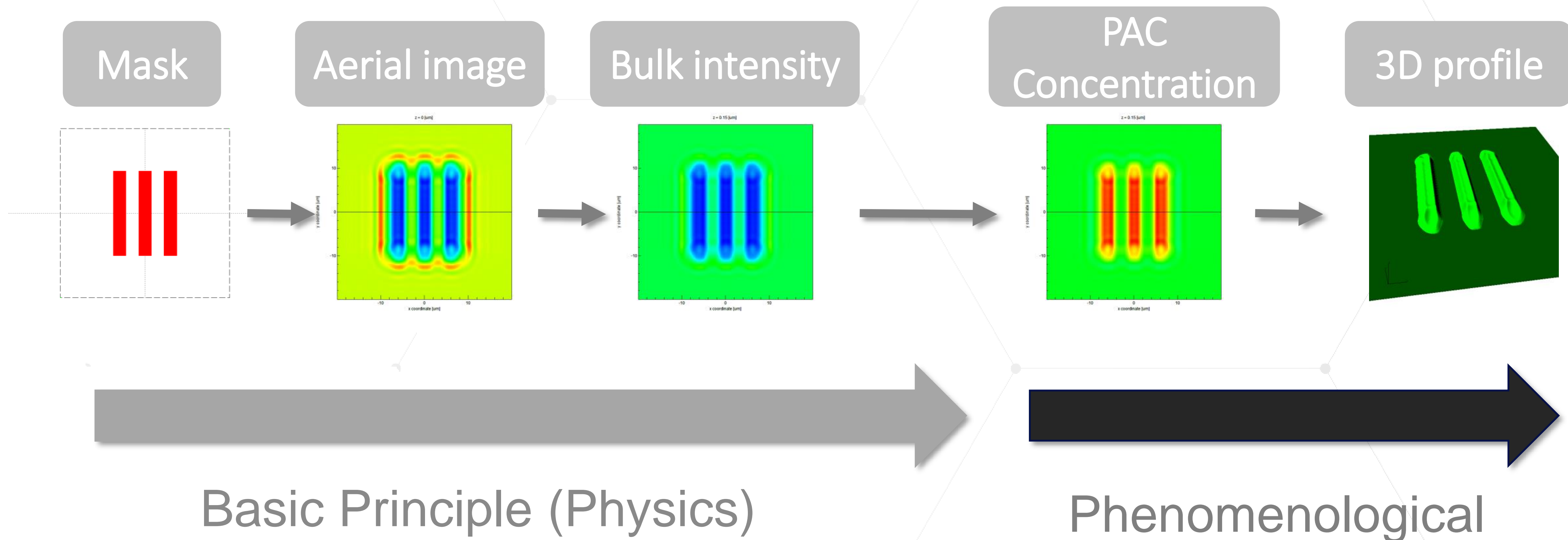


Resist development



LAB

- LAB allows full simulation of projection lithography, including bulk intensity and 3D resist profile.
- In most cases, bulk intensity is enough for exposure analysis.



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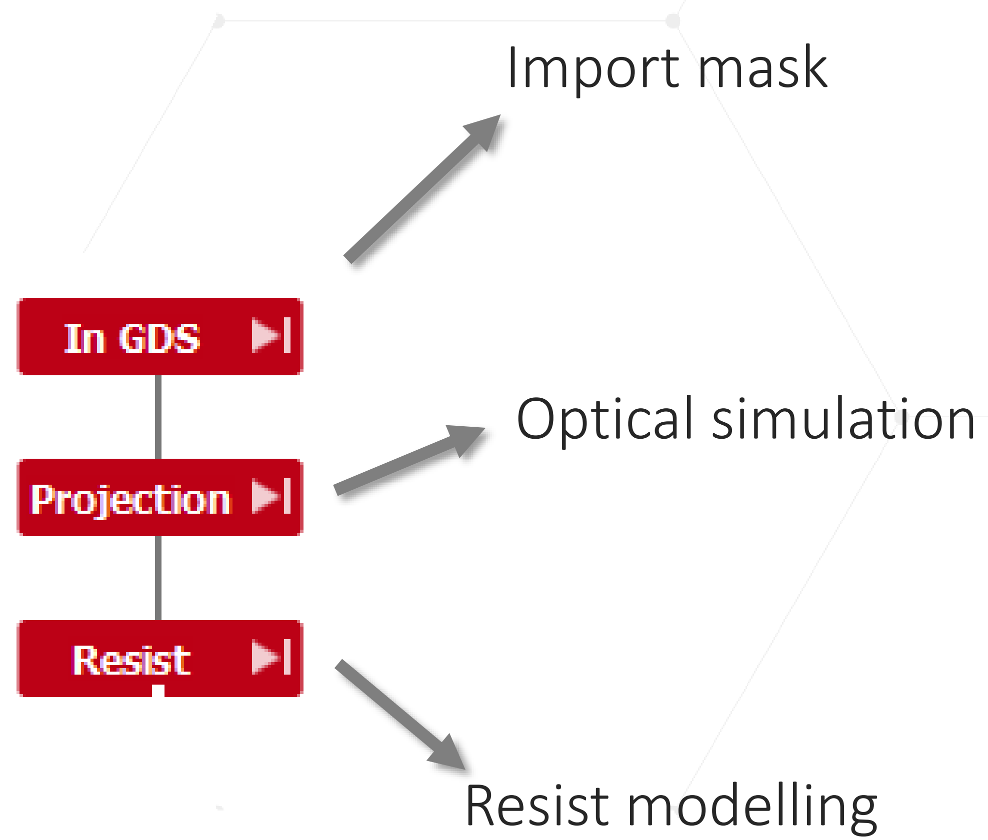
LAB Modelling

- LAB simulation flow:

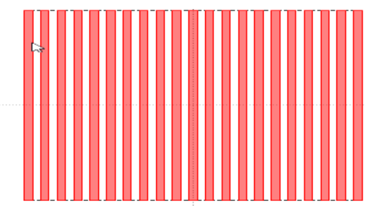


Import mask

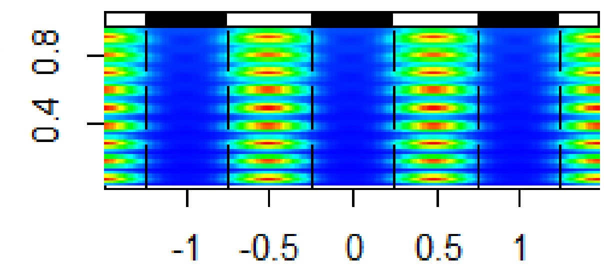
Optical simulation

Resist modelling

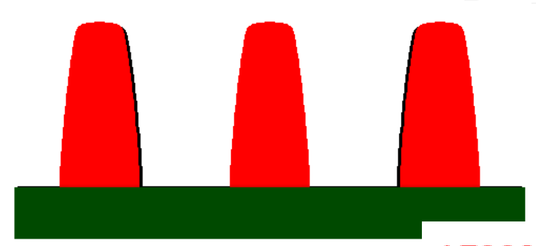
Mask



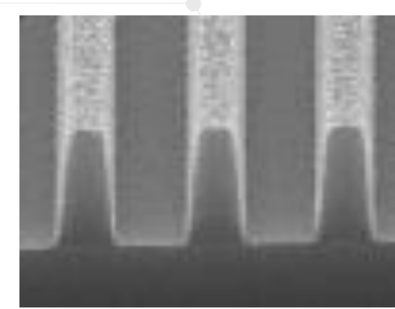
Bulk intensity



Simulated resist profile



SEM image



Outline

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    - Stack Optimization
    - Process Window
    - Resolution Enhancement
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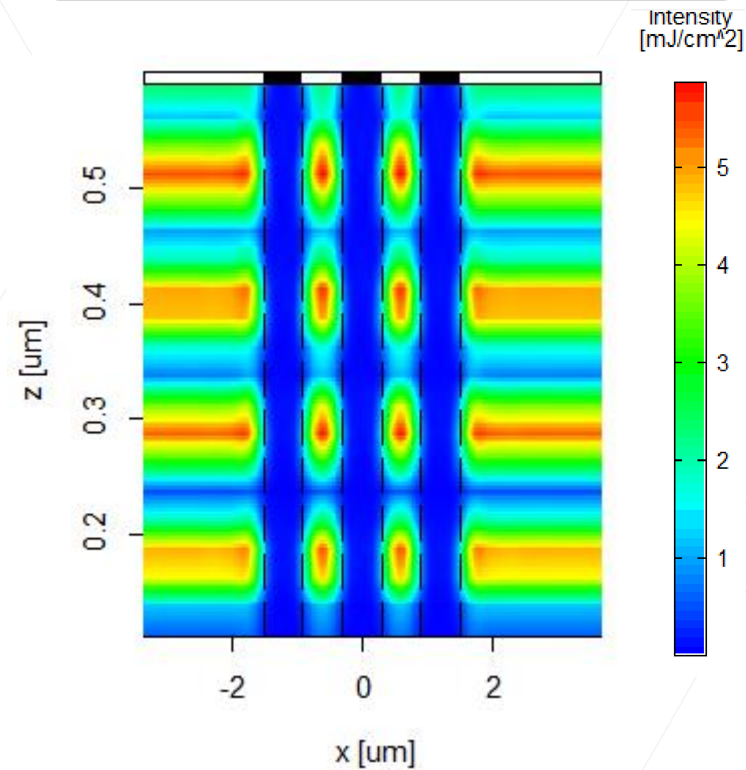
Standing Wave

- Silicon substrate may reflect light strongely back to resist, resulting in process issues.
  - Standing waves cause resist edge roughness

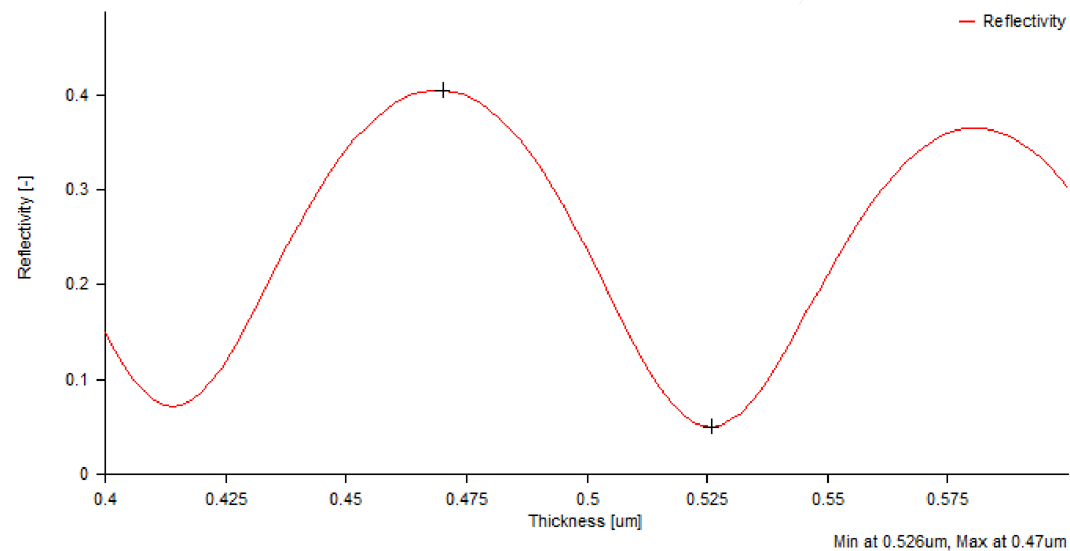
Cross view of bulk image



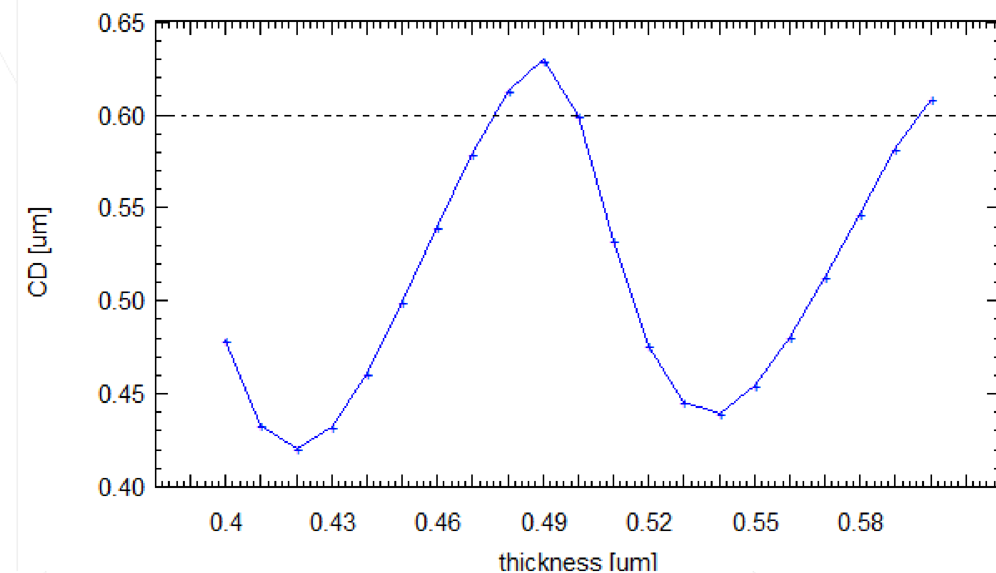
Standing Wave

- Silicon substrate may reflect light strongely back to resist, resulting in process issues:
  - Stack reflectivity is sensitive to resist thickness
  - CD dependence on resist thickness (swing curve)

Stack reflectivity vs resist thickness



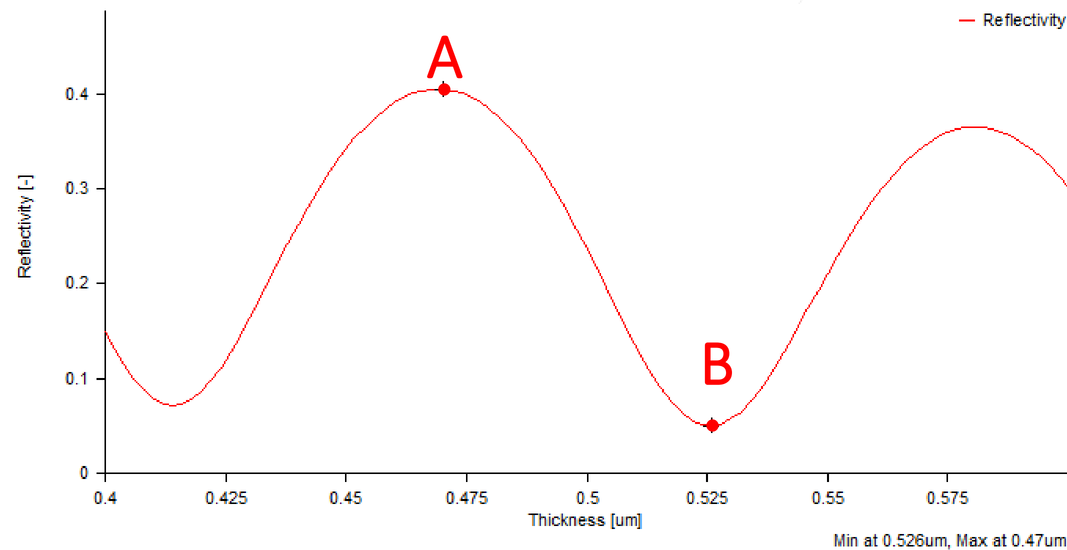
CD Swing curve analysis



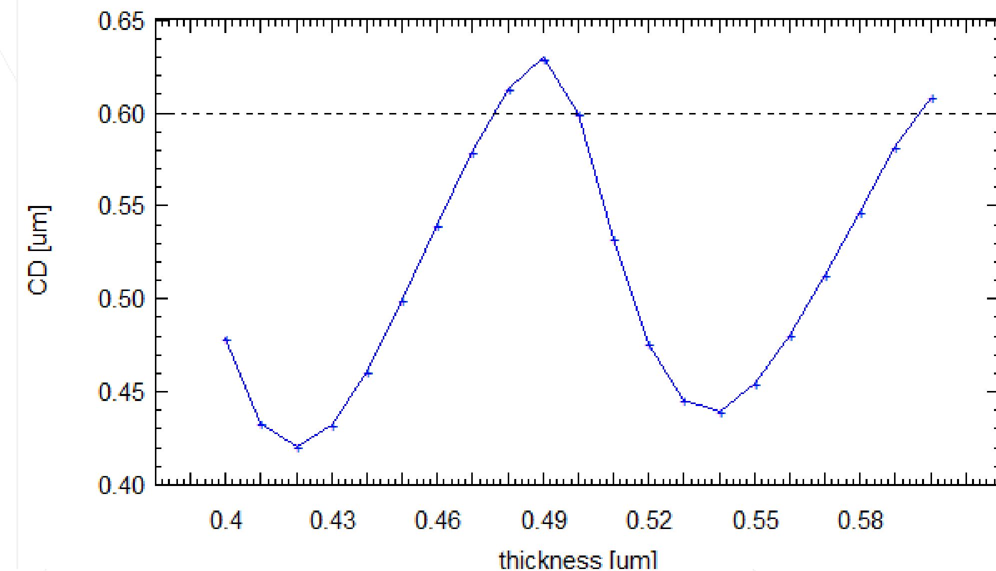
Resist Thickness Optimization

- Silicon substrate may reflect light strongely back to resist, resulting in process sensitivity to resist thickness.
  - Without stack change, the optimum resist thickness is at the top or valley of the reflectivity curve (Position A or B).

Stack reflectivity vs resist thickness



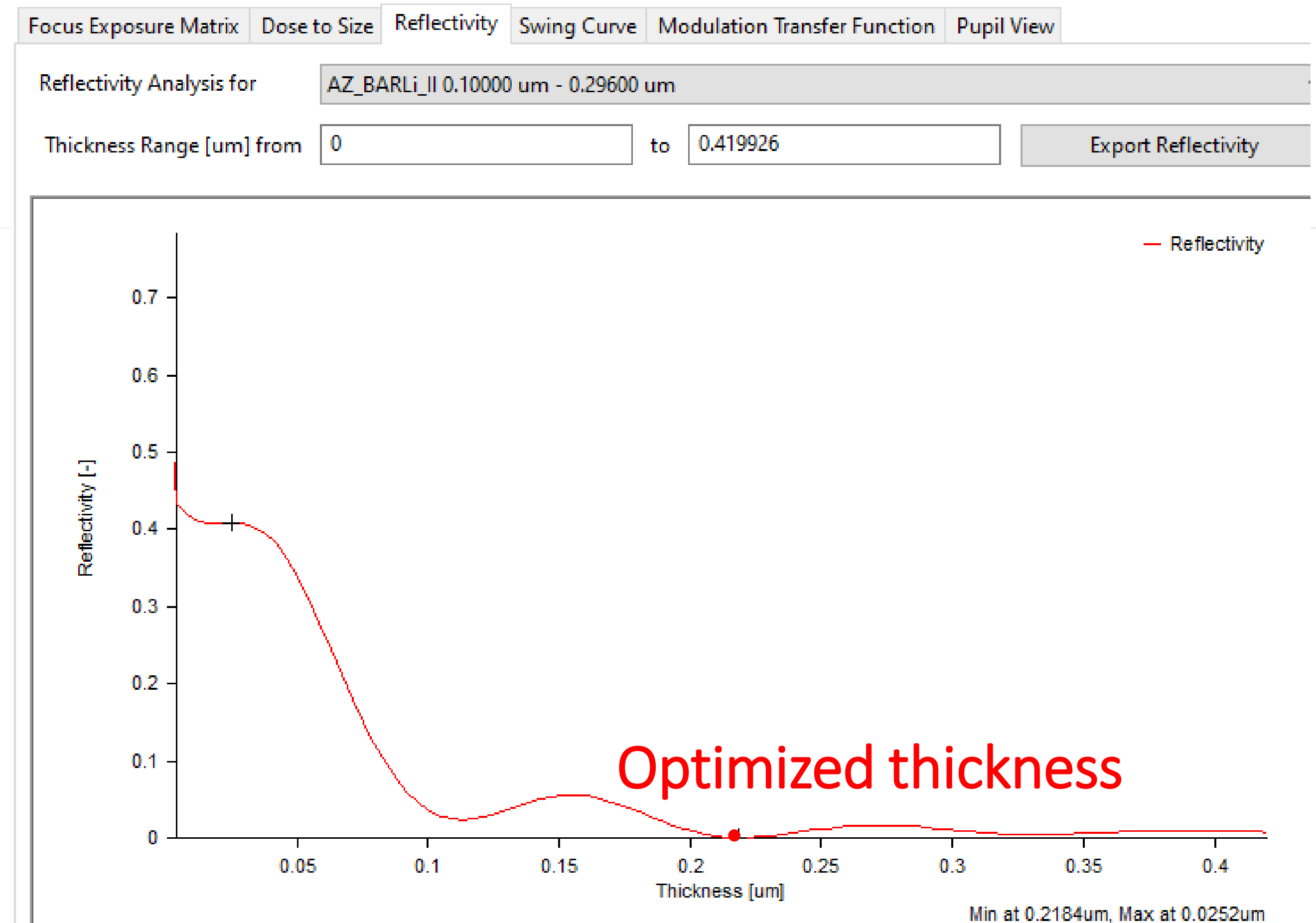
CD Swing curve analysis



Bottom Antireflection Coating

- Bottom antireflection coating (BARC) is widely used to minimize substrate reflection, thus stabilize the process.
  - BARC thickness with the minimum reflection at resist/BARC interface is chosen for BARC layer design.

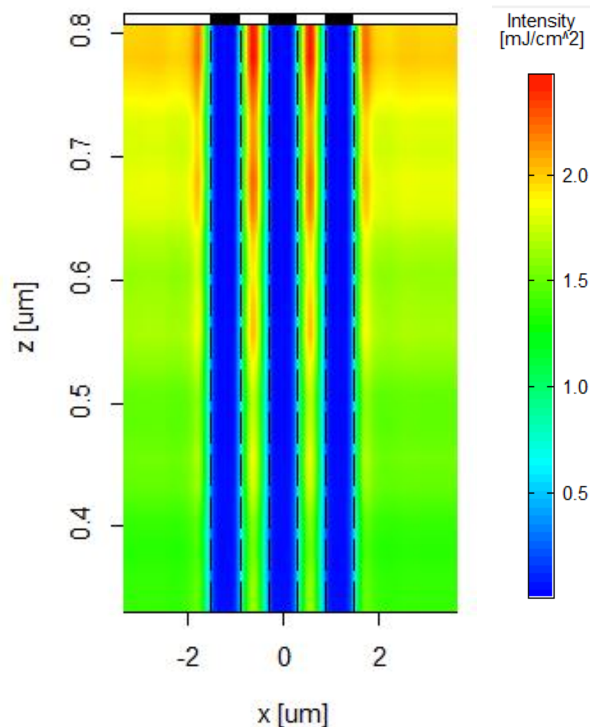
Reflectivity analysis of BARC layer



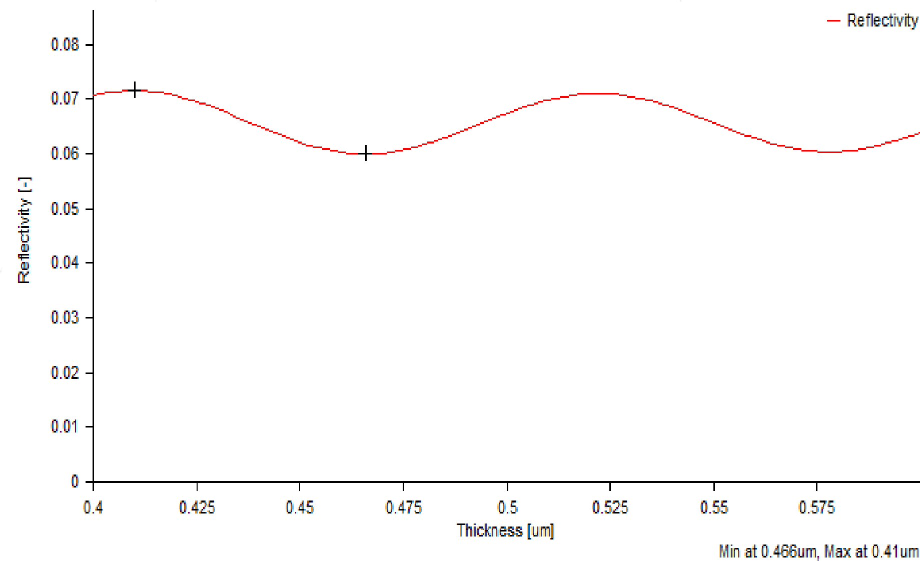
Bottom Antireflection Coating

- Bottom antireflection coating (BARC) is widely used to minimize substrate reflection, thus stabilize the process.
  - With minimized reflection, the CD swing curve shows better process stability to resist thickness.

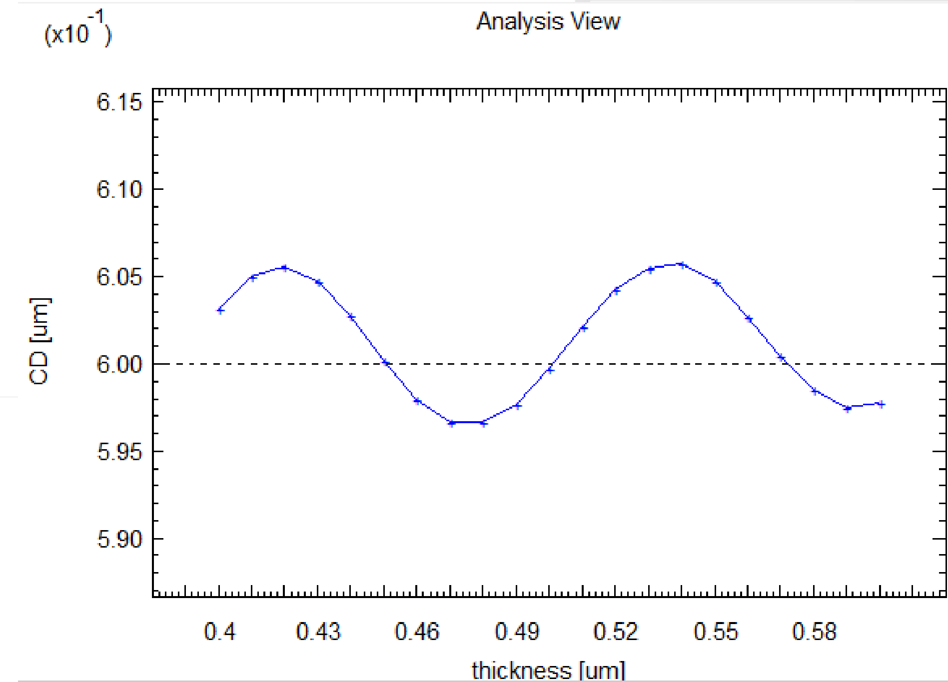
Cross section of bulk image



Stack reflectivity vs resist thickness



CD Swing curve analysis



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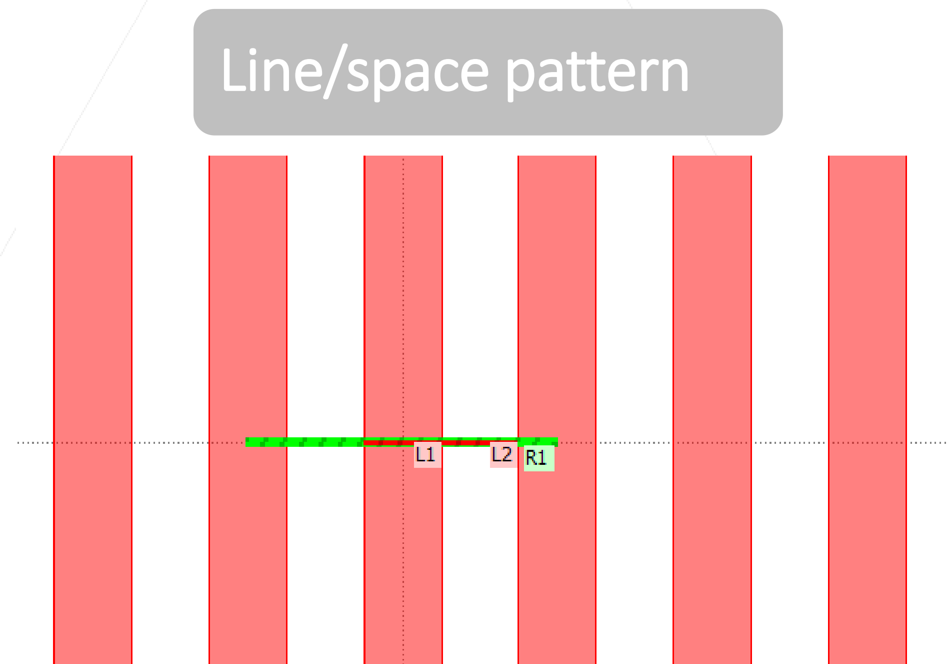
Focus Exposure Matrix Analysis

- Process tolerance with exposure dose and focus position variation is critical for mass production, for which depth of focus and exposure latitude of the process window are important parameters.
- Focus exposure matrix analysis is available in LAB simulation.
- CD and other important features (sidewall angle, etc.) are modeled.
- Two representations: Bossung curve and process window.

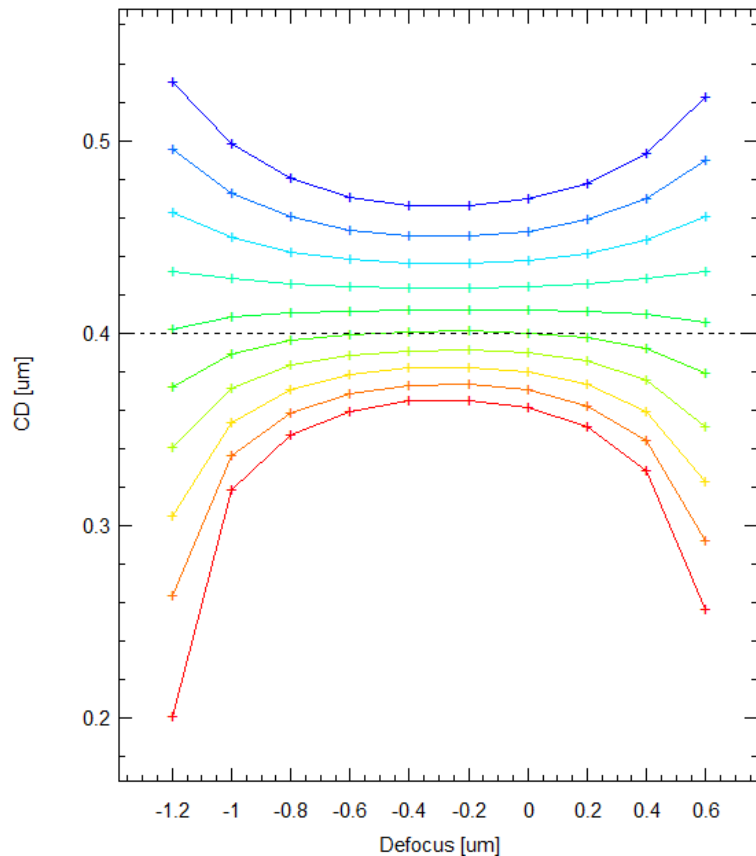
Line/space pattern



Process Window

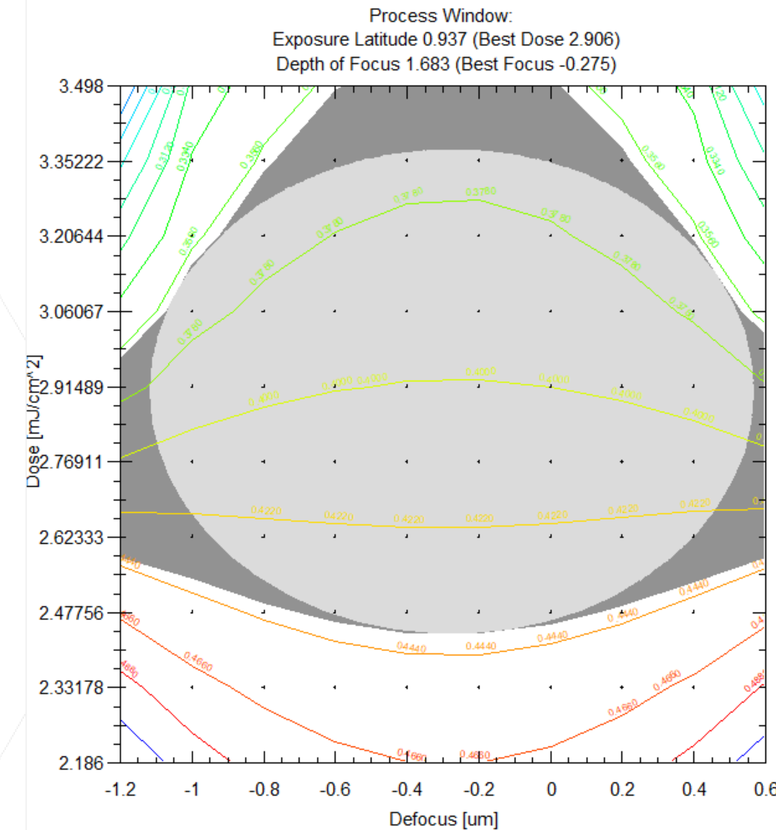
- Bossung curve shows the CD variation with dose and defocus.
- Process window defines the dose and defocus range with accepted CD size.

Bossung curve



dose
2.2
3.5

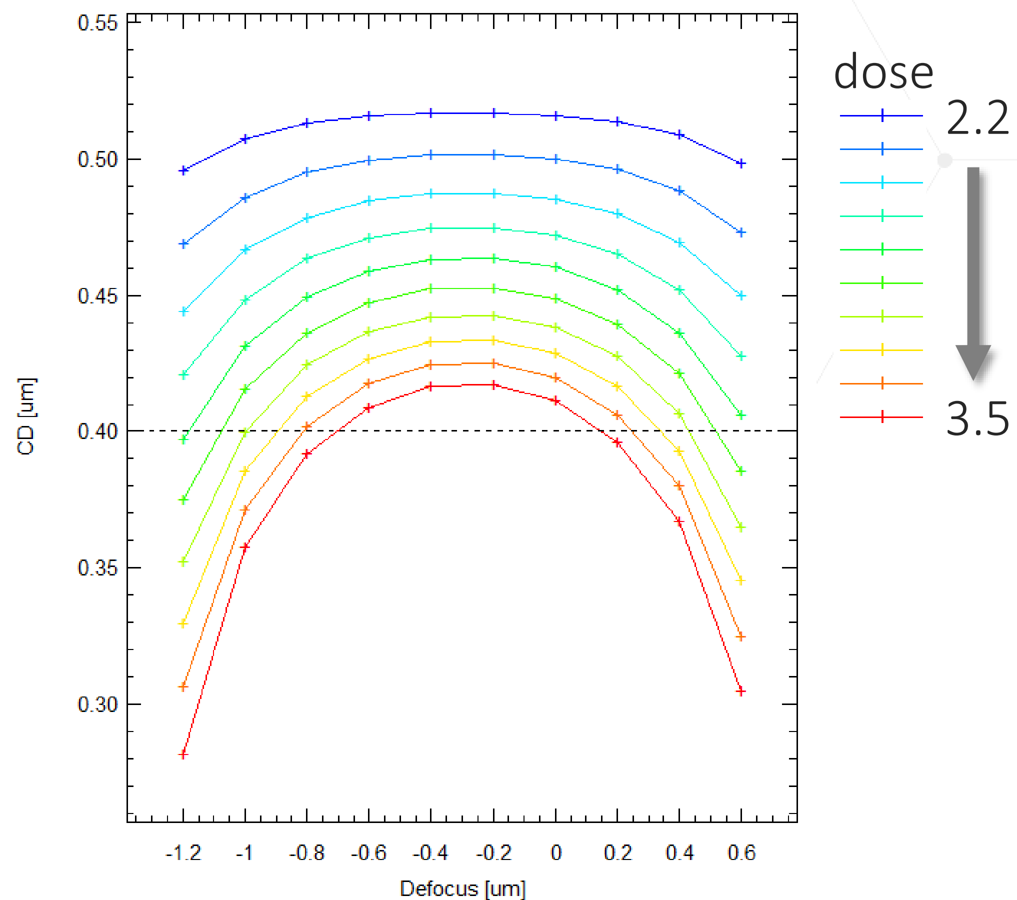
Process window



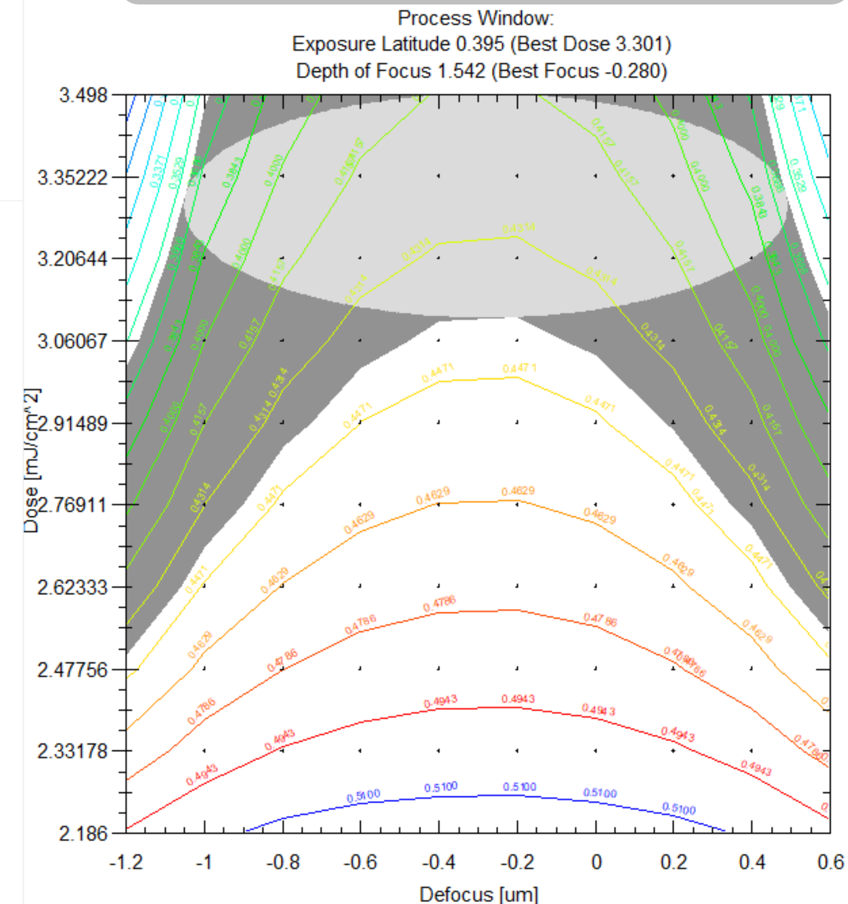
Process Window

- For application cases with a big variation of pattern density, the process window for low pattern density (isoline) may also be simulated.

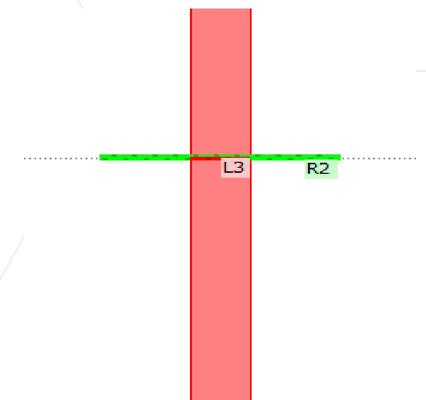
Bossung curve for isoline



Process window for isoline



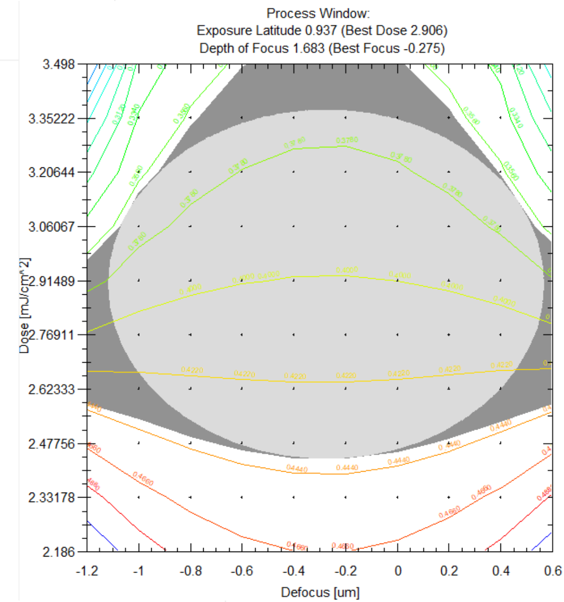
Isoline pattern



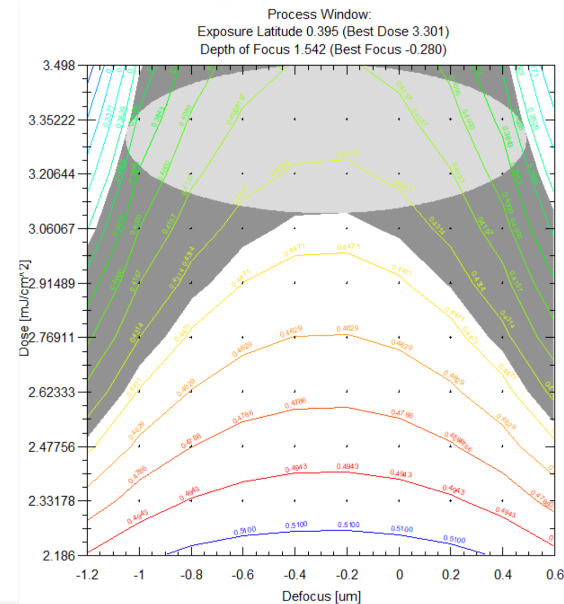
Process Window Overlap

- Overlaped process window achieves that of various pattern densities.

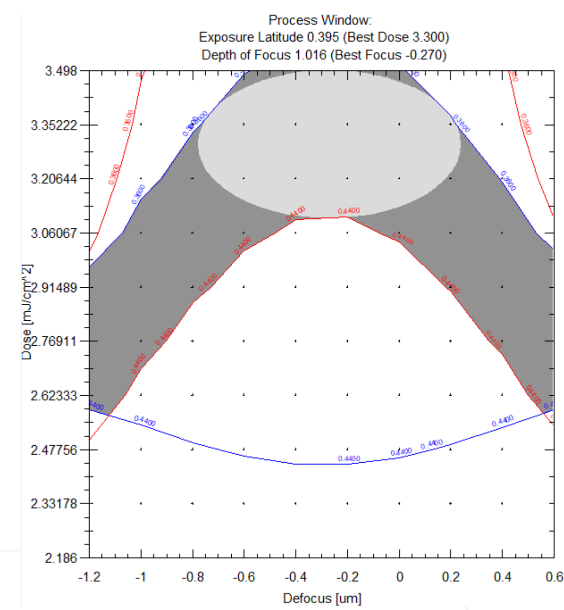
Process window for dense line



Process window for isoline



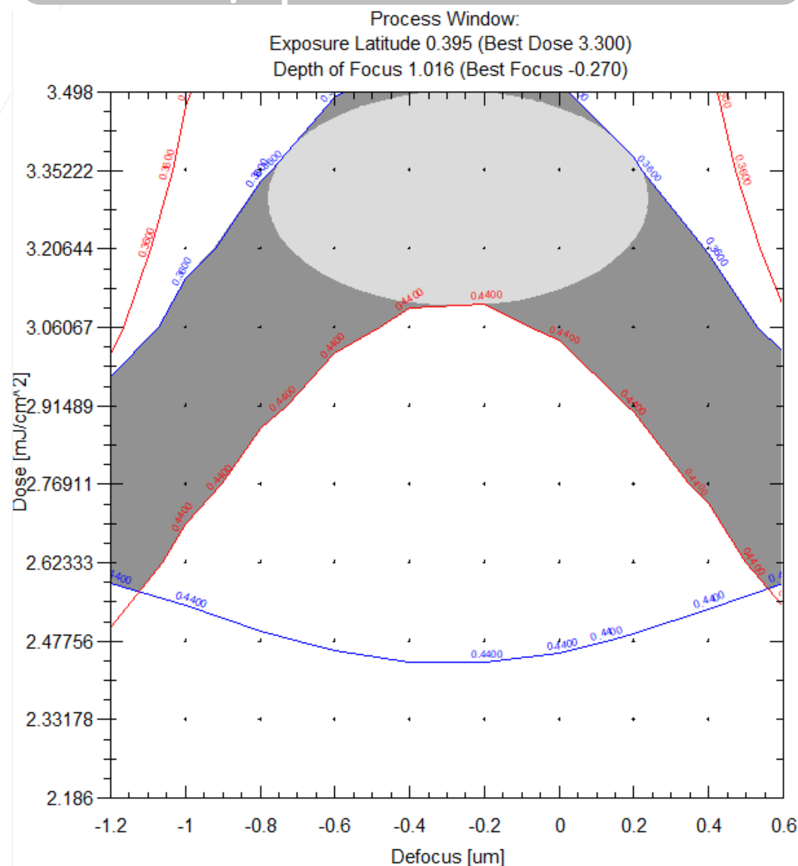
Process window overlap



Process Window Restrictions

- The process window is adjusted by adding restrictions, according to fabrication limits.

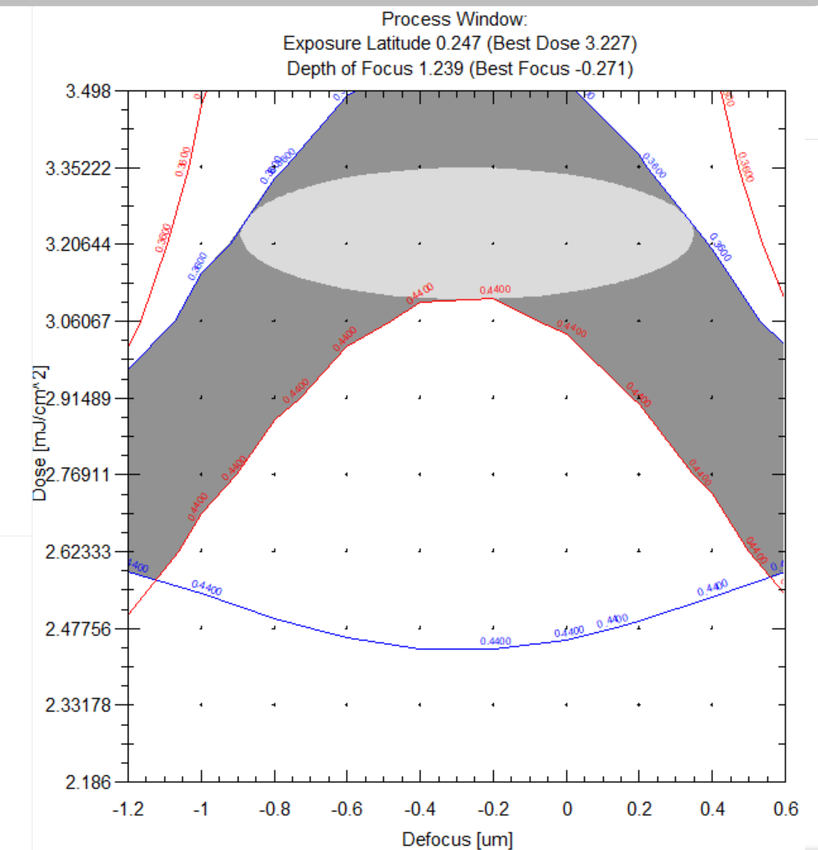
Process window overlap for line/space and isoline



Process window restriction

☑ Minimum width	1.2	
☐ Minimum height	0.000000	
☐ Center Xmin and Xmax	0.000000	0.000000
☐ Center Ymin and Ymax	0.000000	0.000000

Proces window with restriction



Process Window for Resist

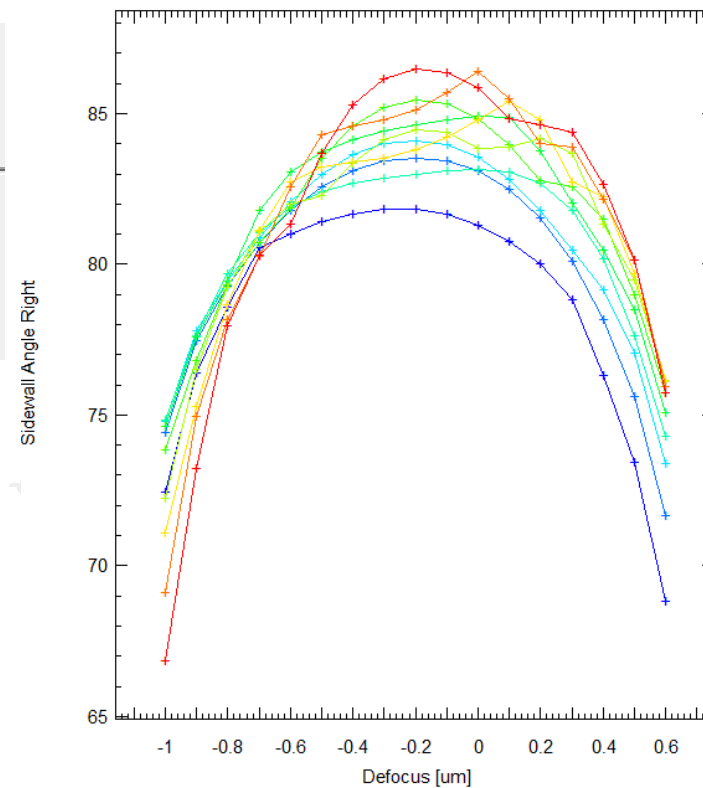
- Except CD, process window analysis is available for resist profile related features, like sidewall angle, resist height, etc..

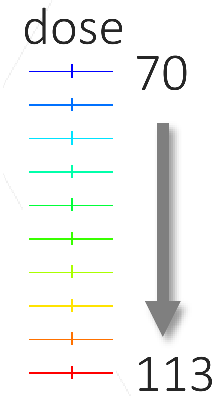
Feature selection

Group Filter
☐ Bottom ☐ Center
☐ Top ☑ BulkImage

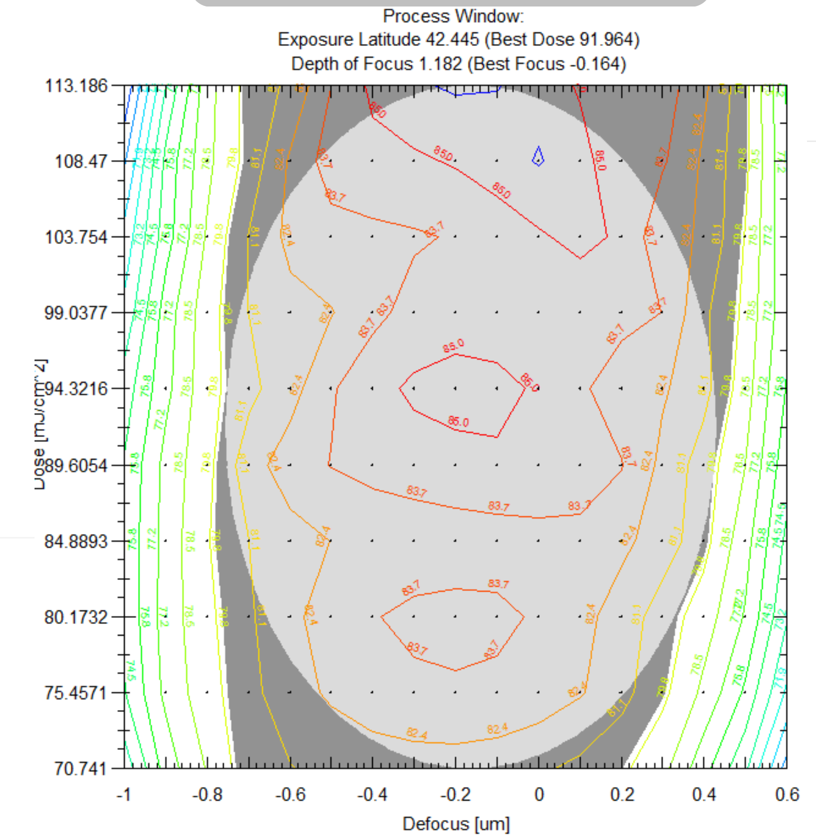
Measure Filter
☑ CD ☐ Sidewall Angle Left
☑ Sidewall Angle Right ☐ Resist Height
☐ Resist Loss ☐ CSE

Bossung curve





Process window



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Resolution Enhancement

- Photolithography transfers the pattern via optical imaging.
- The optical imaging limits the resolution of the pattern transfer.
- With the demands of smaller and smaller feature size, techniques have been applied to improve the resolution.
  - Optical proximity correction (OPC) via mask modification
  - Source optimization
  - Other techniques, e.g. phase shift mask

Grating Fabrication

- A grating with 200 nm feature size is designed. KrF projection exposure is expected to be able to fabricate it.
- The LAB simulation shows the inaccuracy of exposure: line shortening, corner rounding.

Bragg grating design

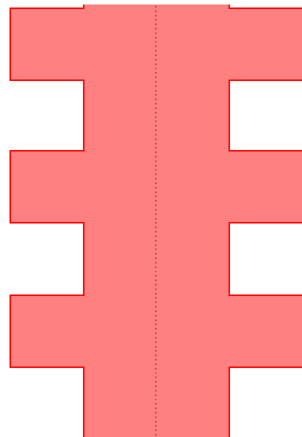


Image in resist

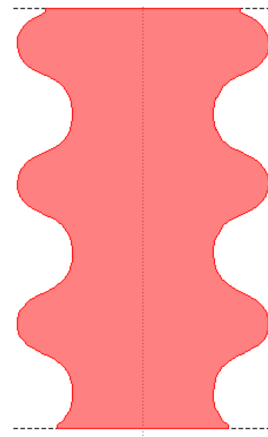
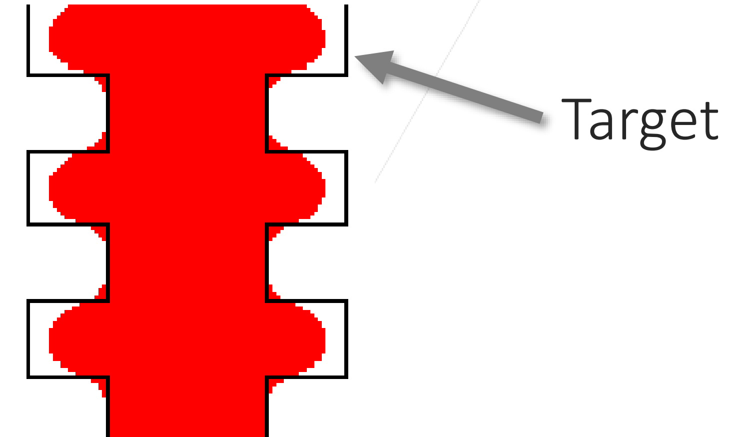
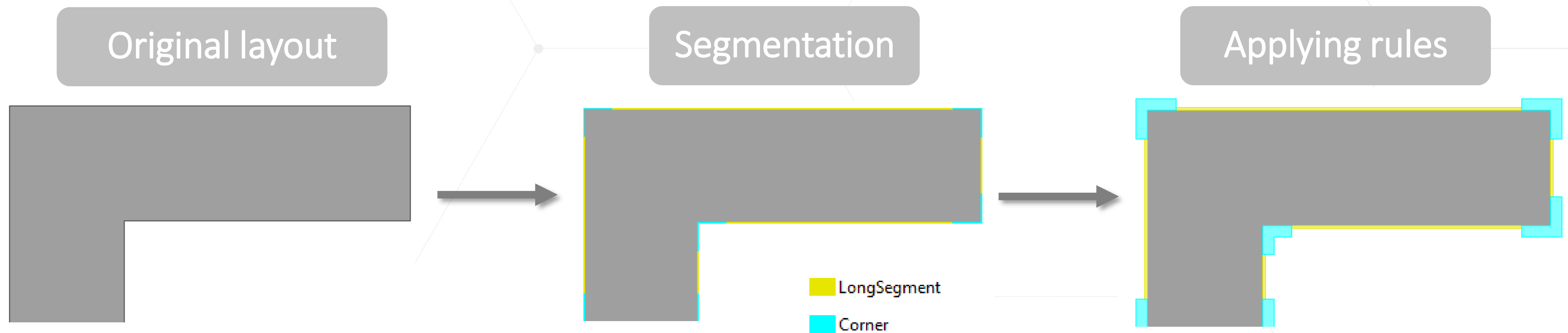


Image overlay with design



Rule OPC

- Rule-OPC allows user to correct the pattern as user wishes.
- The working procedure for rule-OPC:
  - The layout is first split into segments.
  - Each segment is modified depending on the user defined rules.
  - OPC rules can be previewed and analyzed in the Rule OPC panel.



Rule OPC

- Rule OPC modifies the mask by applying rules at various segments.
- The serif at the inner corner minimizes the corner rounding issue and serif at the outer corner solve the line end shortening issue.
- Rule OPC shows its flexibility for pattern with simple shapes.

Pattern after rule OPC

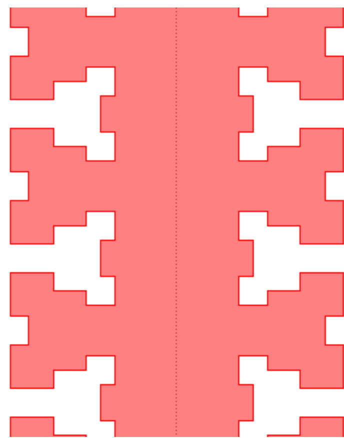


Image in resist

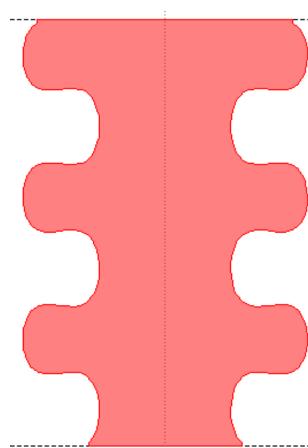
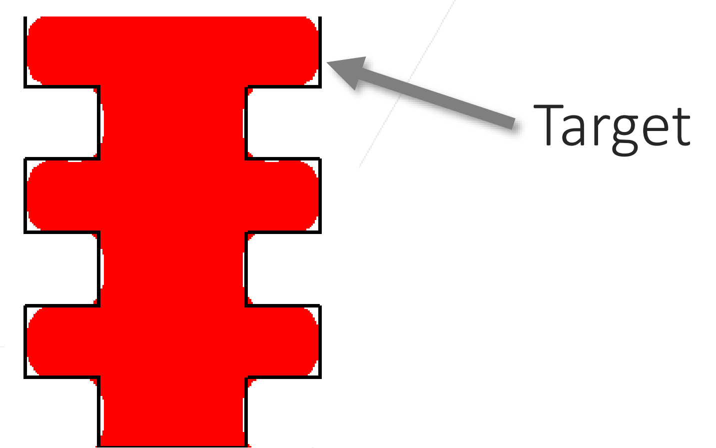
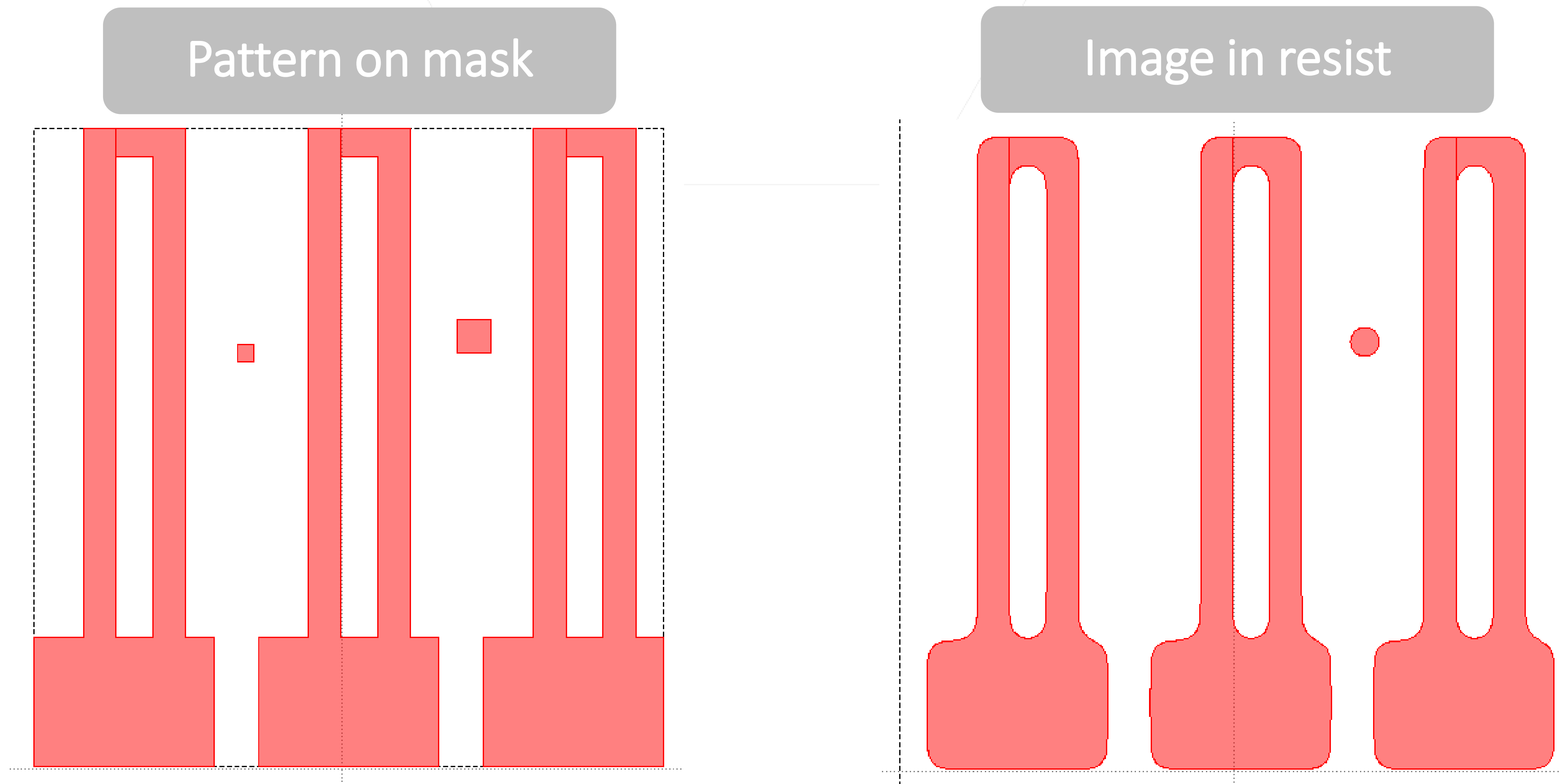


Image overlay with design



Pattern Fidelity

- The following example shows pattern fidelity problem of a complex pattern: corner rounding, feature missing, etc..



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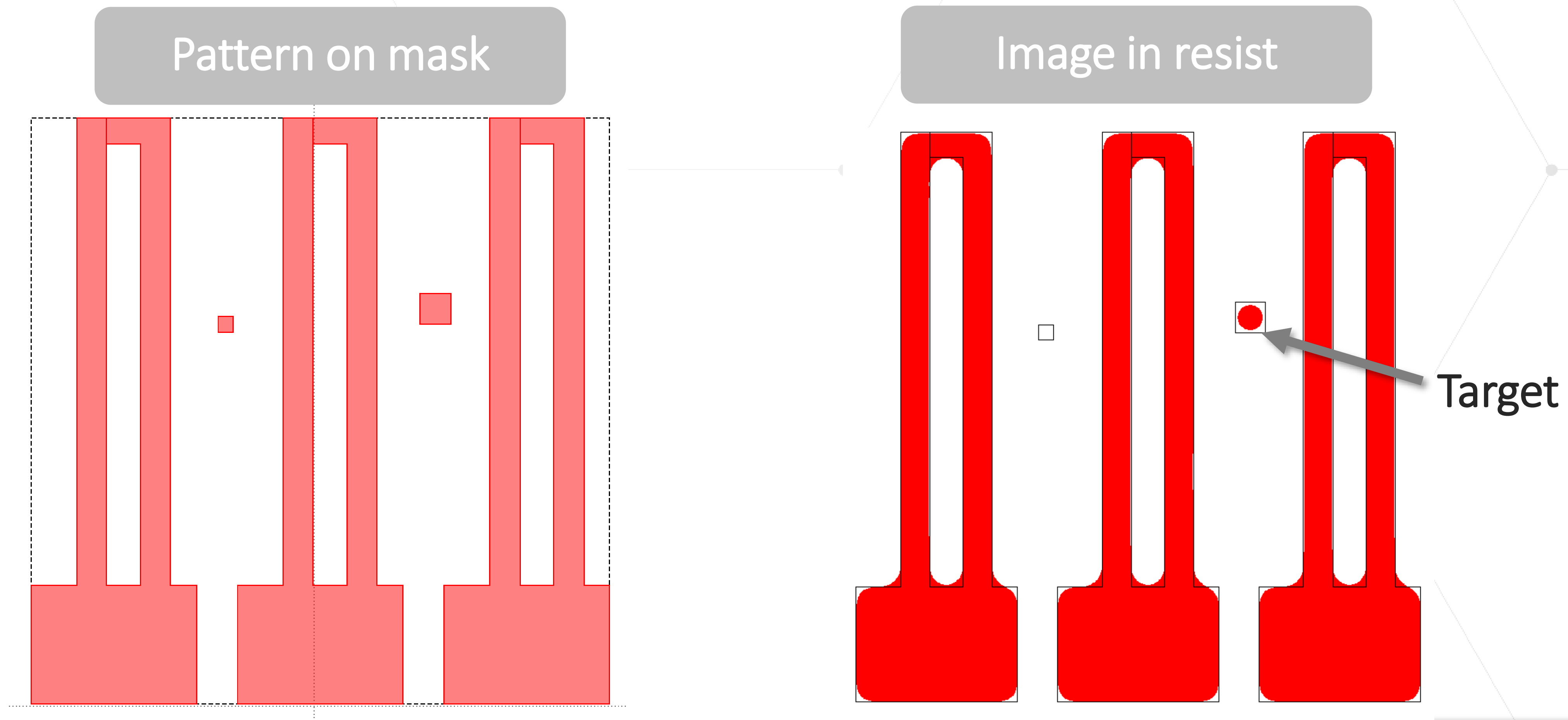
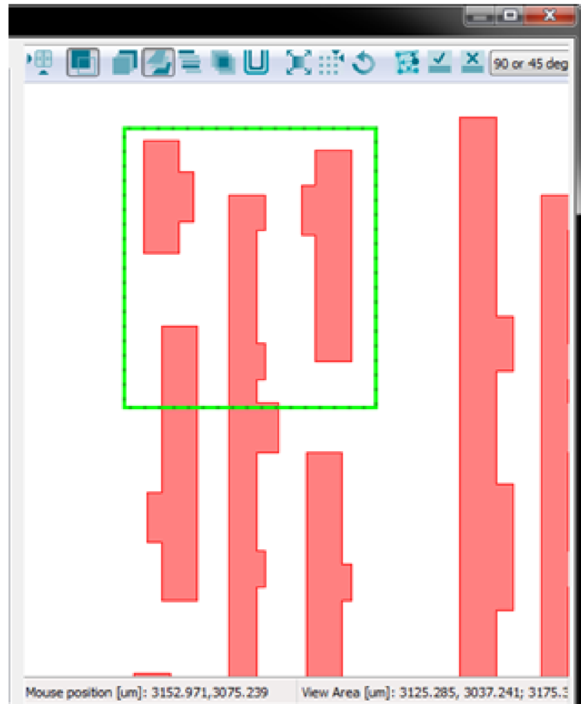
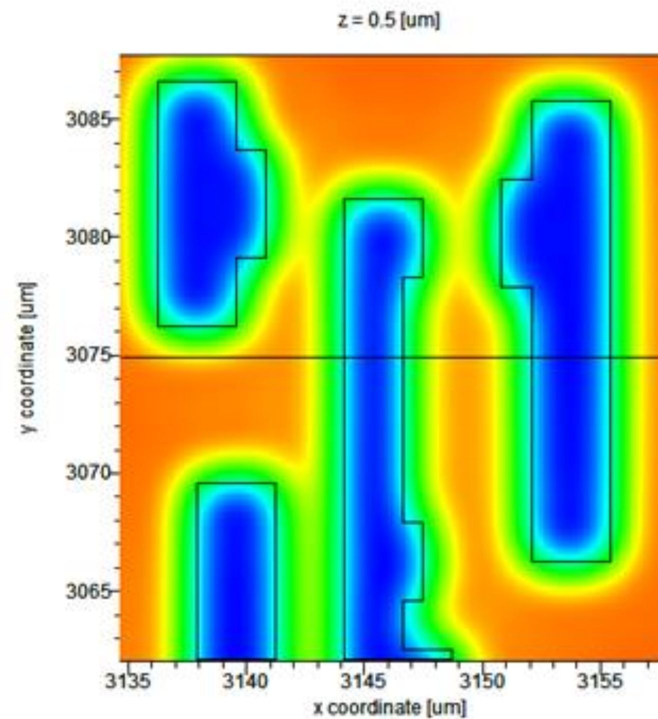


Model OPC

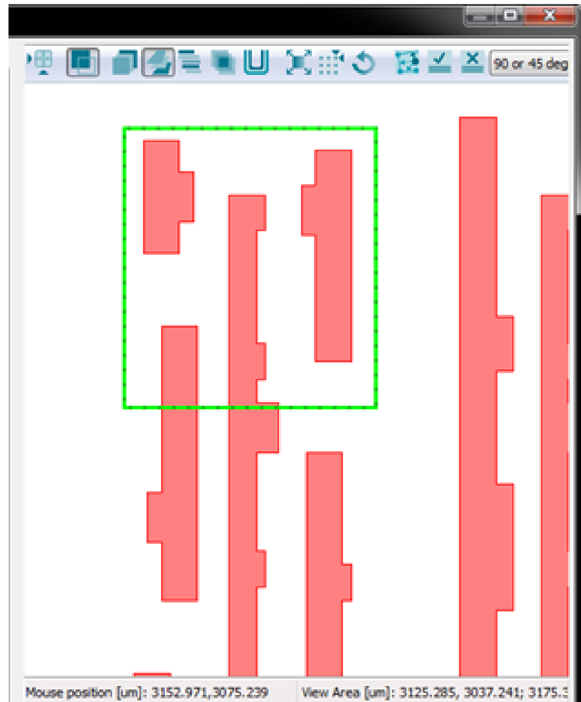


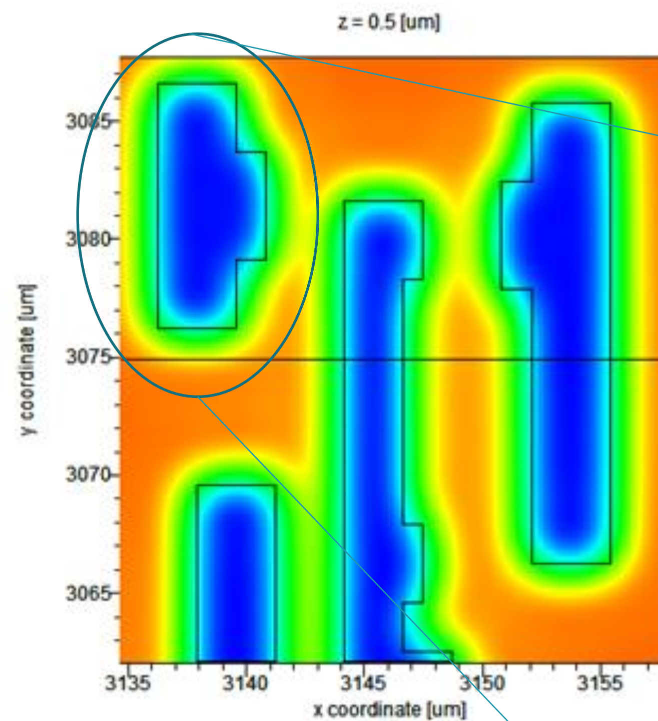


Fully automated correction:

- Iterative process
- The exposure is modelled at layout edges (fast simulation)

Model OPC





Fully automated correction:

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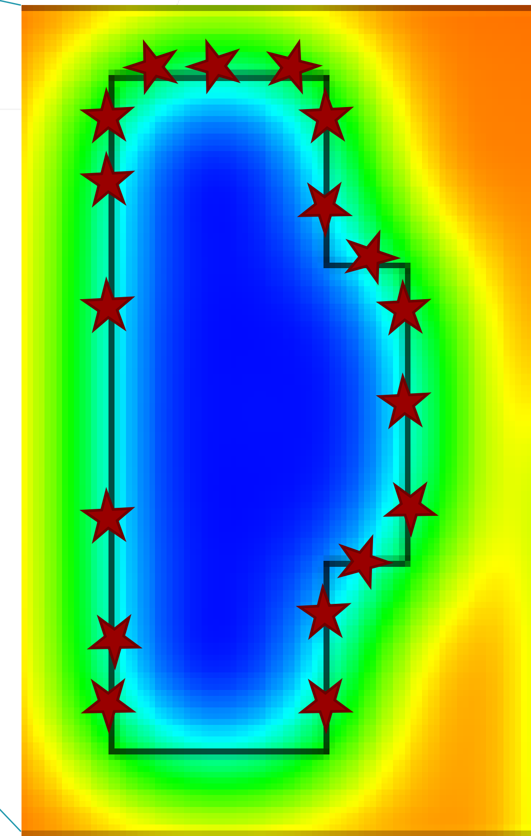
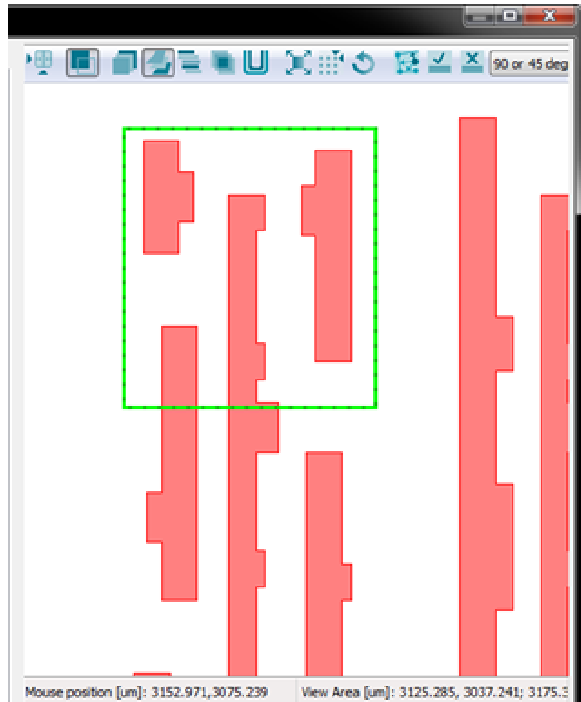
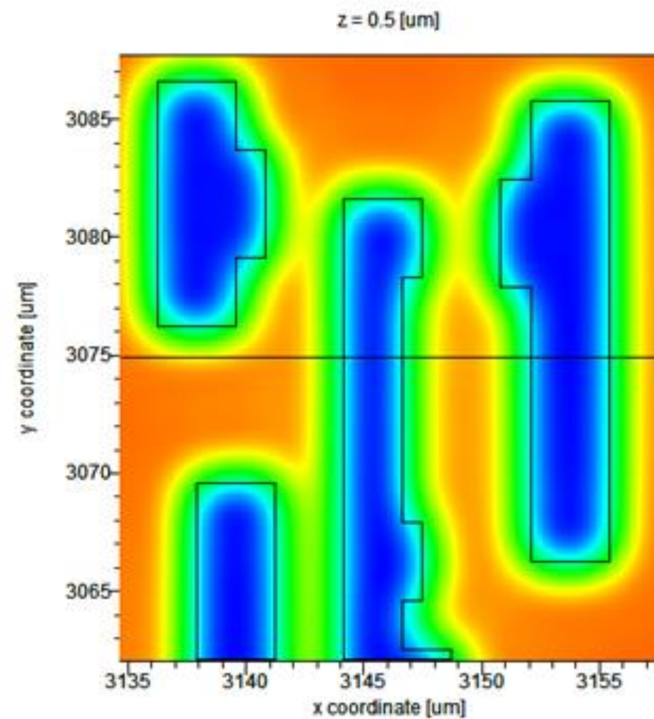
- The exposure is modelled at layout edges (fast simulation)



- Placing of evaluation points at layout edge
- Compare intensity level
  - at taget: no action
  - Below or above target: move edges

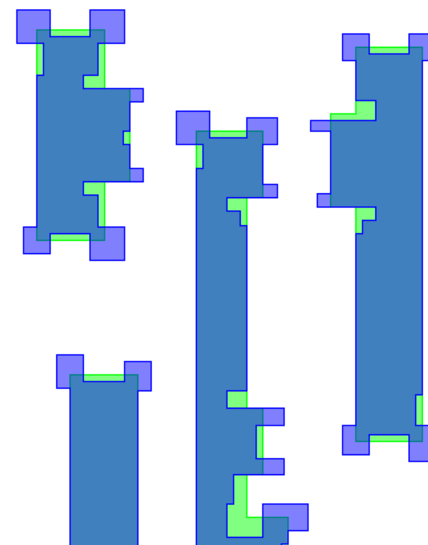
Model OPC





Fully automated correction:

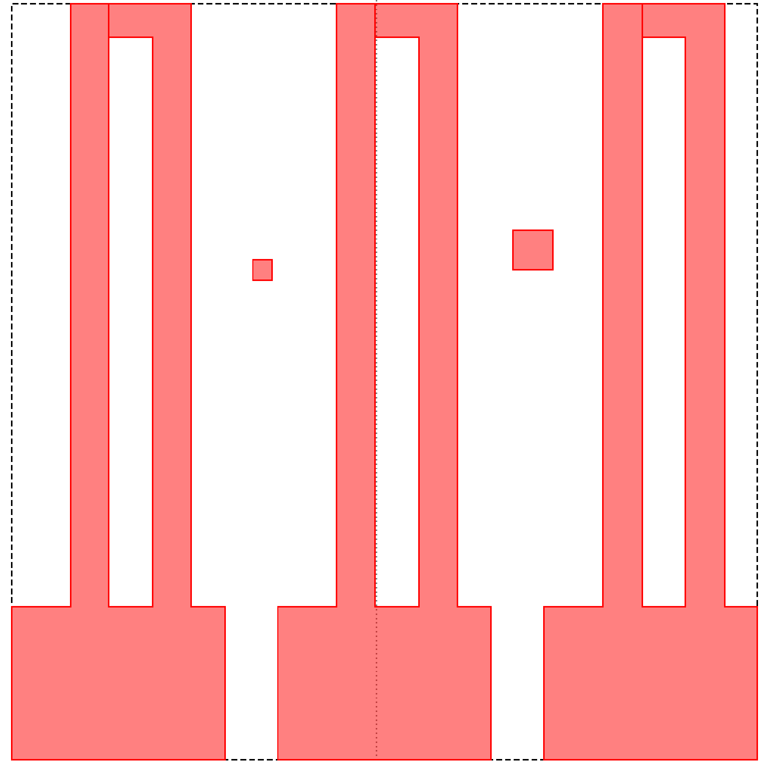
- Iterative process
- The exposure is modelled at layout edges (fast simulation), compared to target
- the layout is modified (shape correction) to compensate for mismatch
- Full layout import



Model-OPC

- In comparison, the pattern after model-OPC shows compensation at the corners.
- The pattern fidelity has been enhanced in corners and small features.

Pattern on mask



Pattern after model OPC

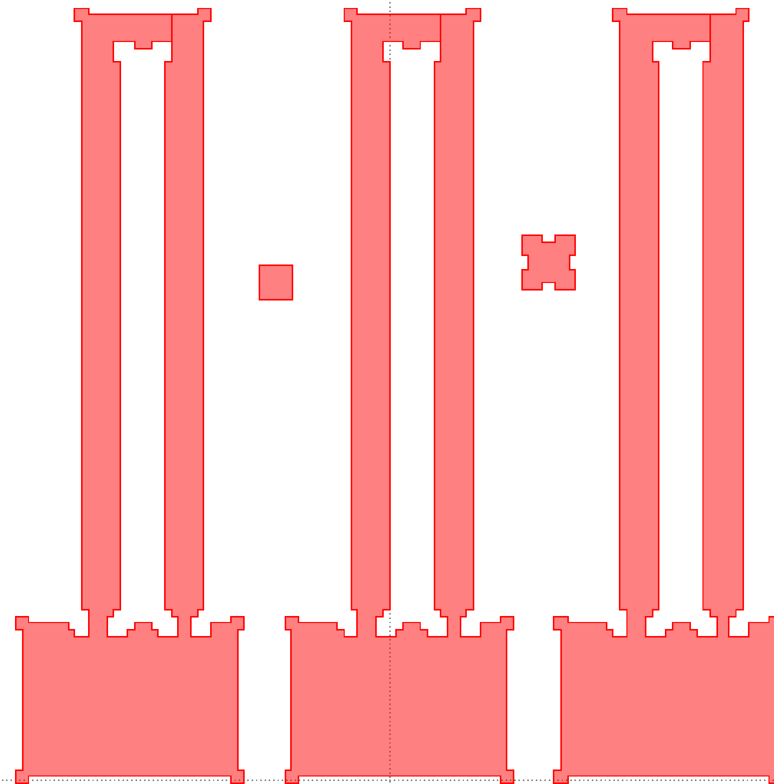
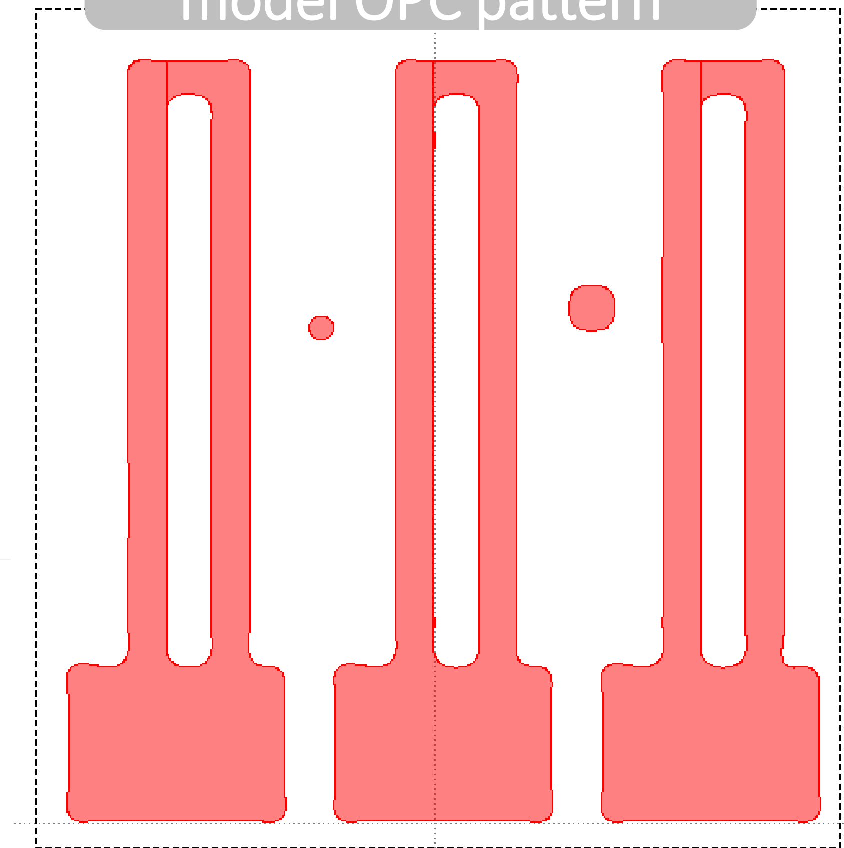


Image in resist for model OPC pattern



Model-OPC

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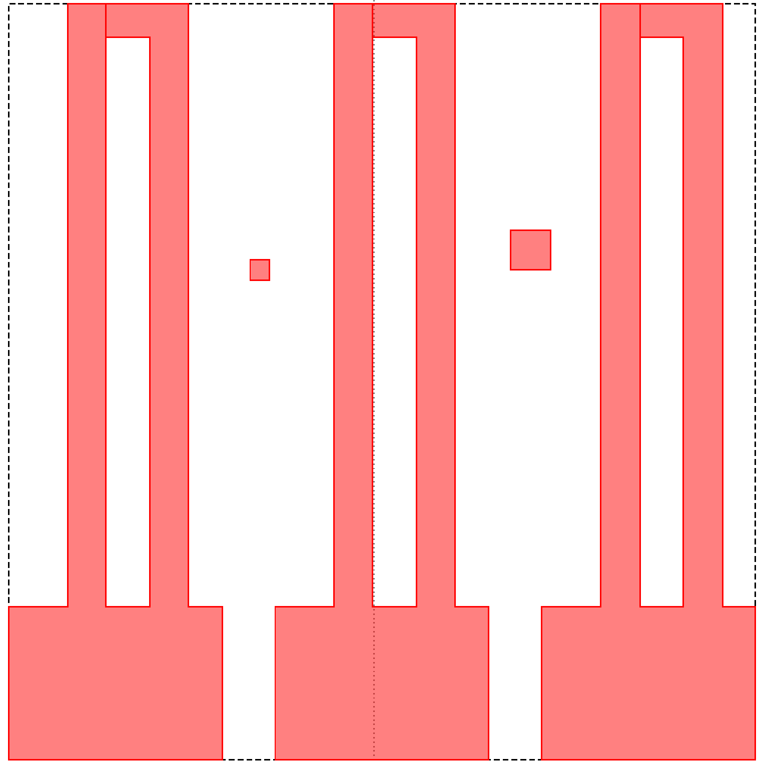
Pattern on mask



Pattern after model OPC

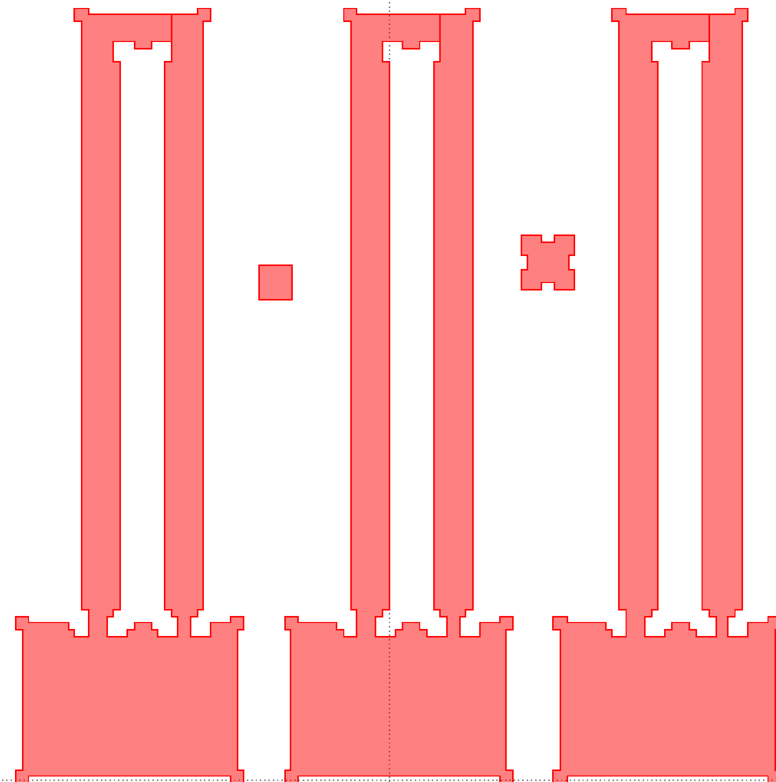
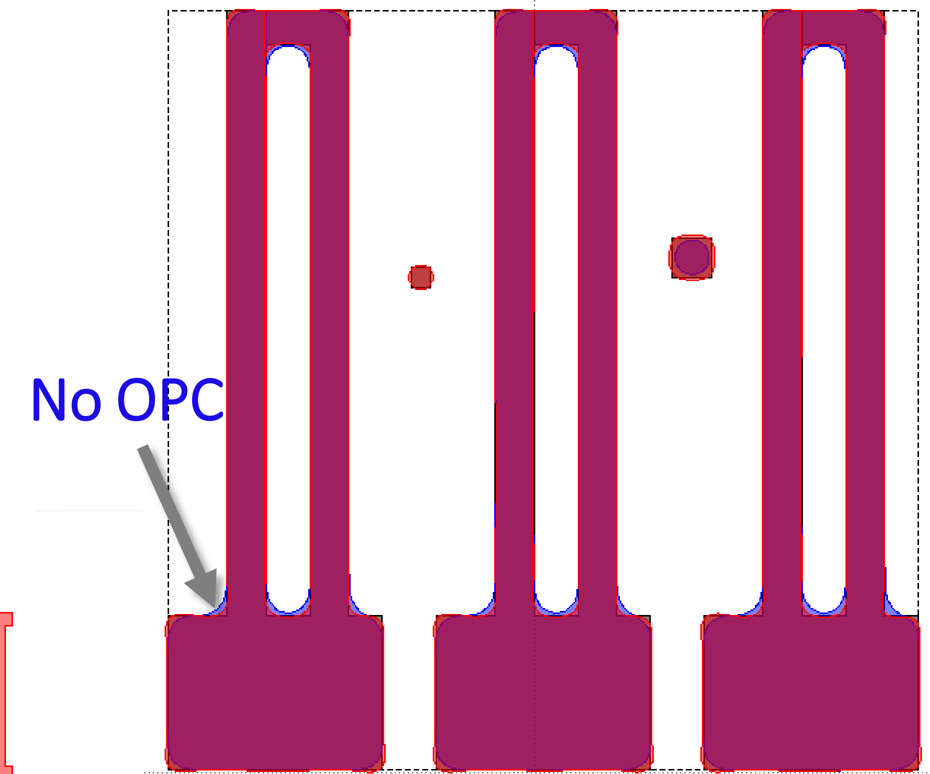


Image in resist for model OPC pattern



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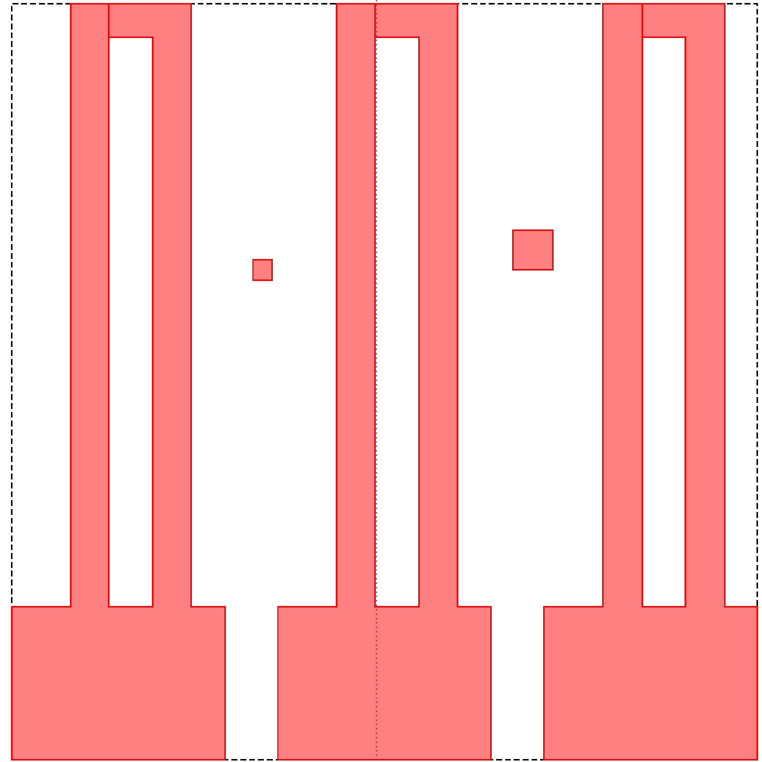
Pattern on mask



Pattern after model OPC

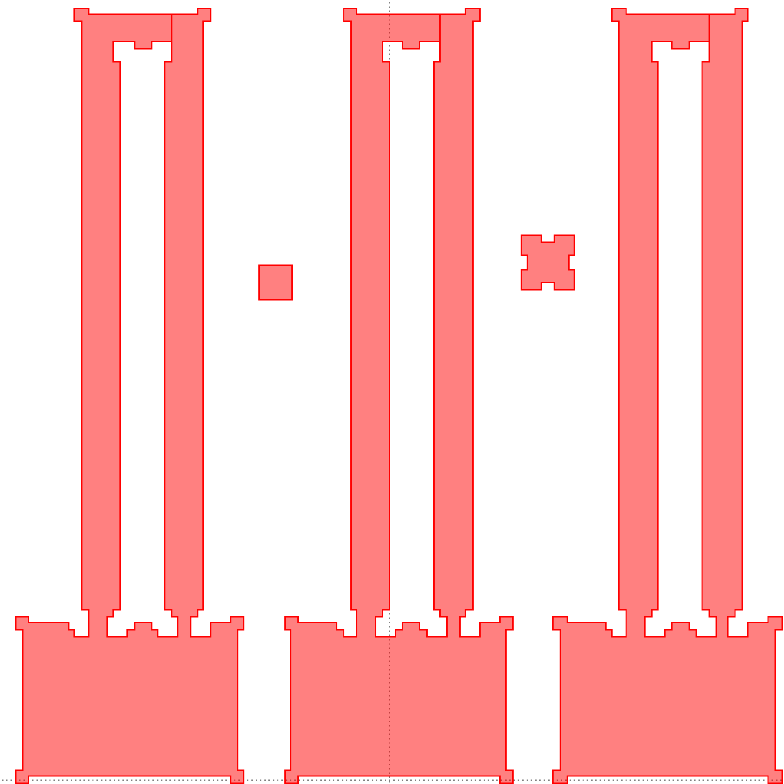
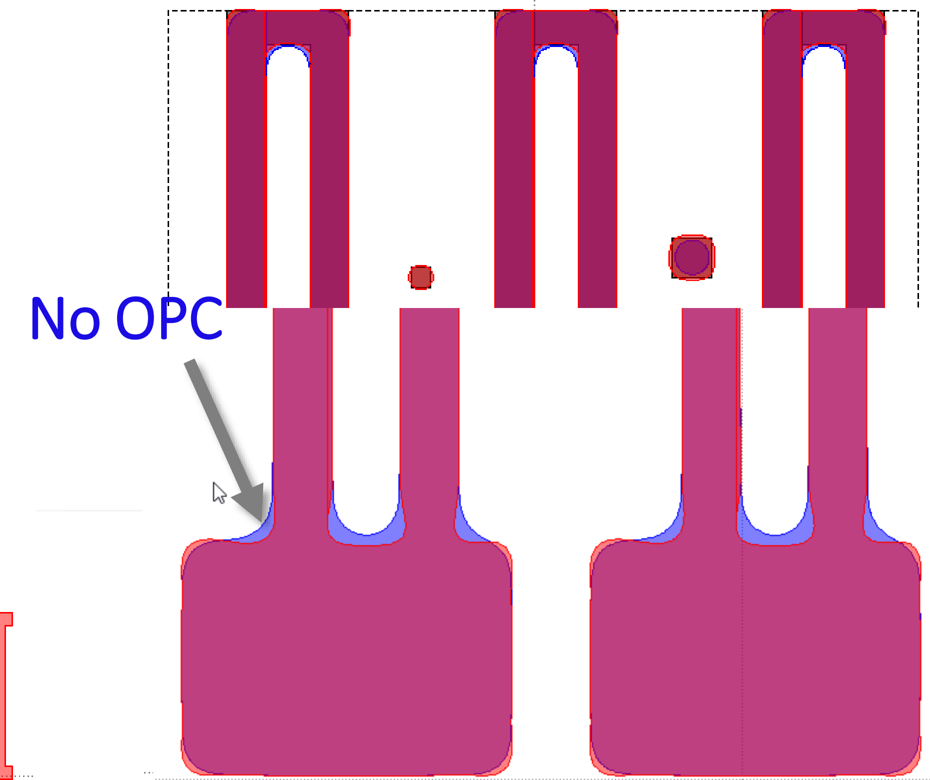
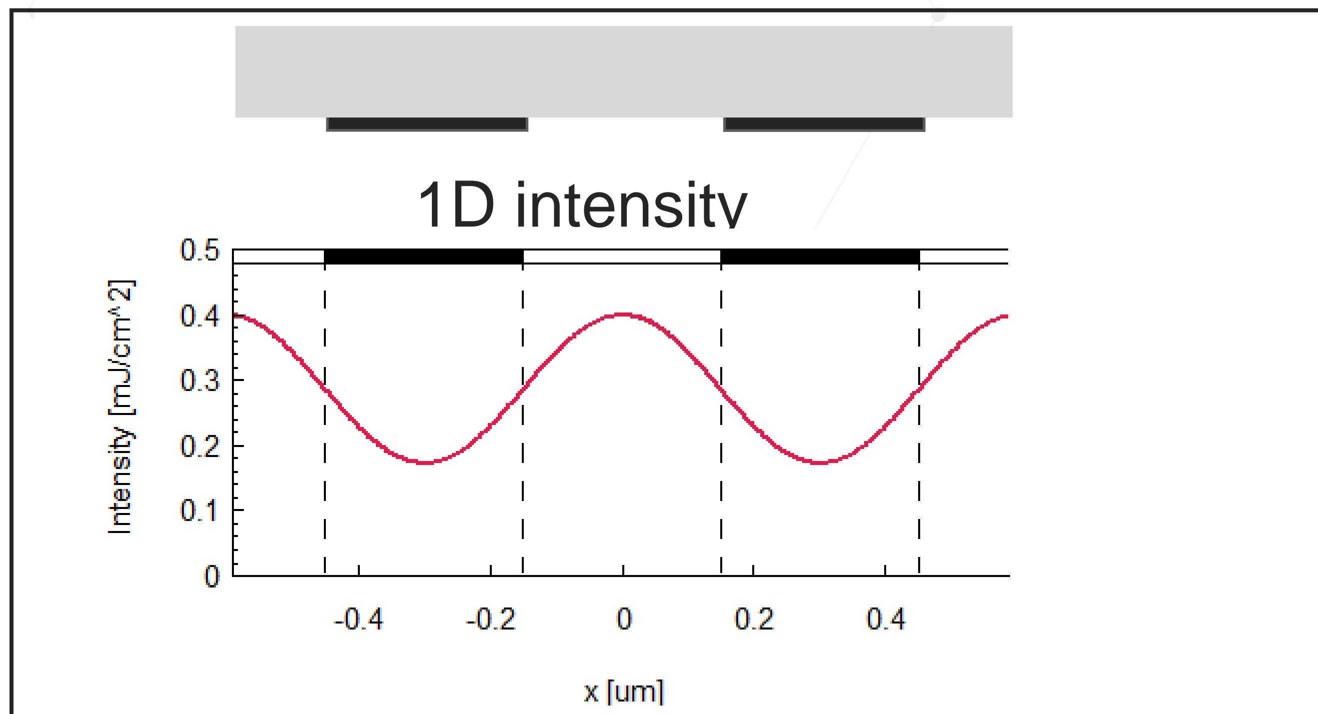


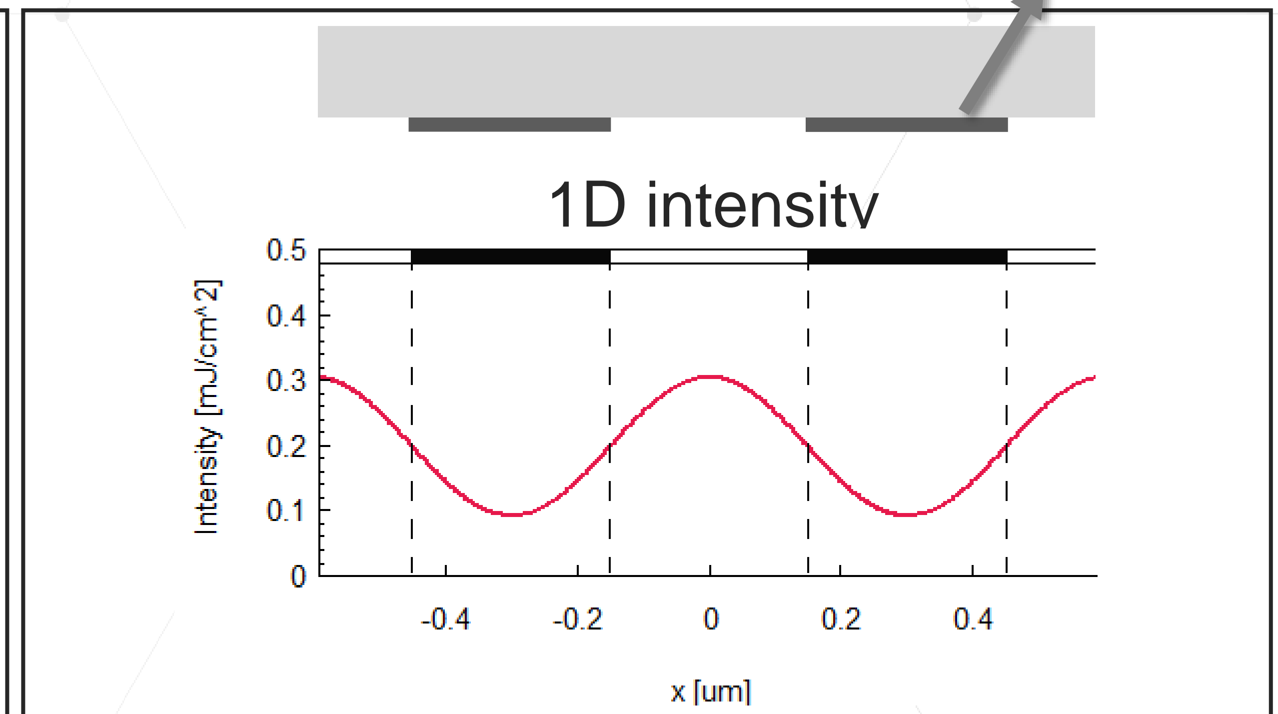
Image in resist for model OPC pattern



Attenuated Phase Shift Mask

- To improve the resolution, attenuated phase shift mask (PSM) is one technique.
  - Attenuated PSM has 180° phase shift from the space and a small transmission (e.g. 6%)



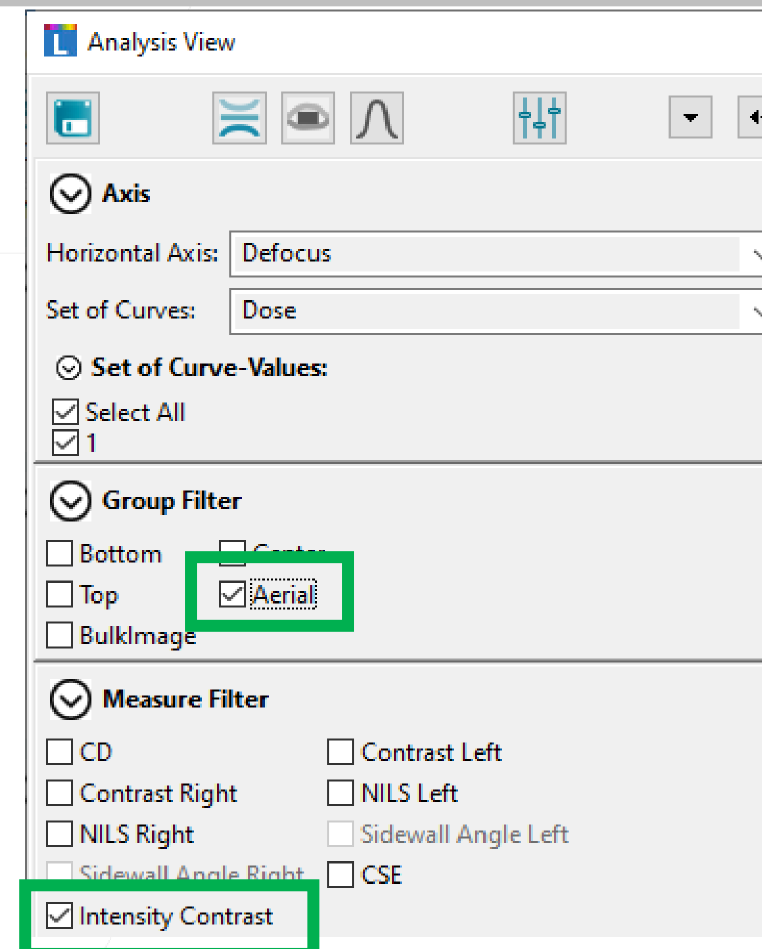


Aerial Image Analysis

- The quality of aerial image decides the subsequent exposure and controls the final resist profile.
- LAB simulates the aerial image and provides user access to classical merit of image quality:
  - image contrast
  - image log slope.

Image contrast = $\frac{I_{max}-I_{min}}{I_{max}+I_{min}}$

Image contrast in analysis view



Aerial Image Analysis

- The quality of aerial image decides the subsequent exposure quality and controls the final resist profile.
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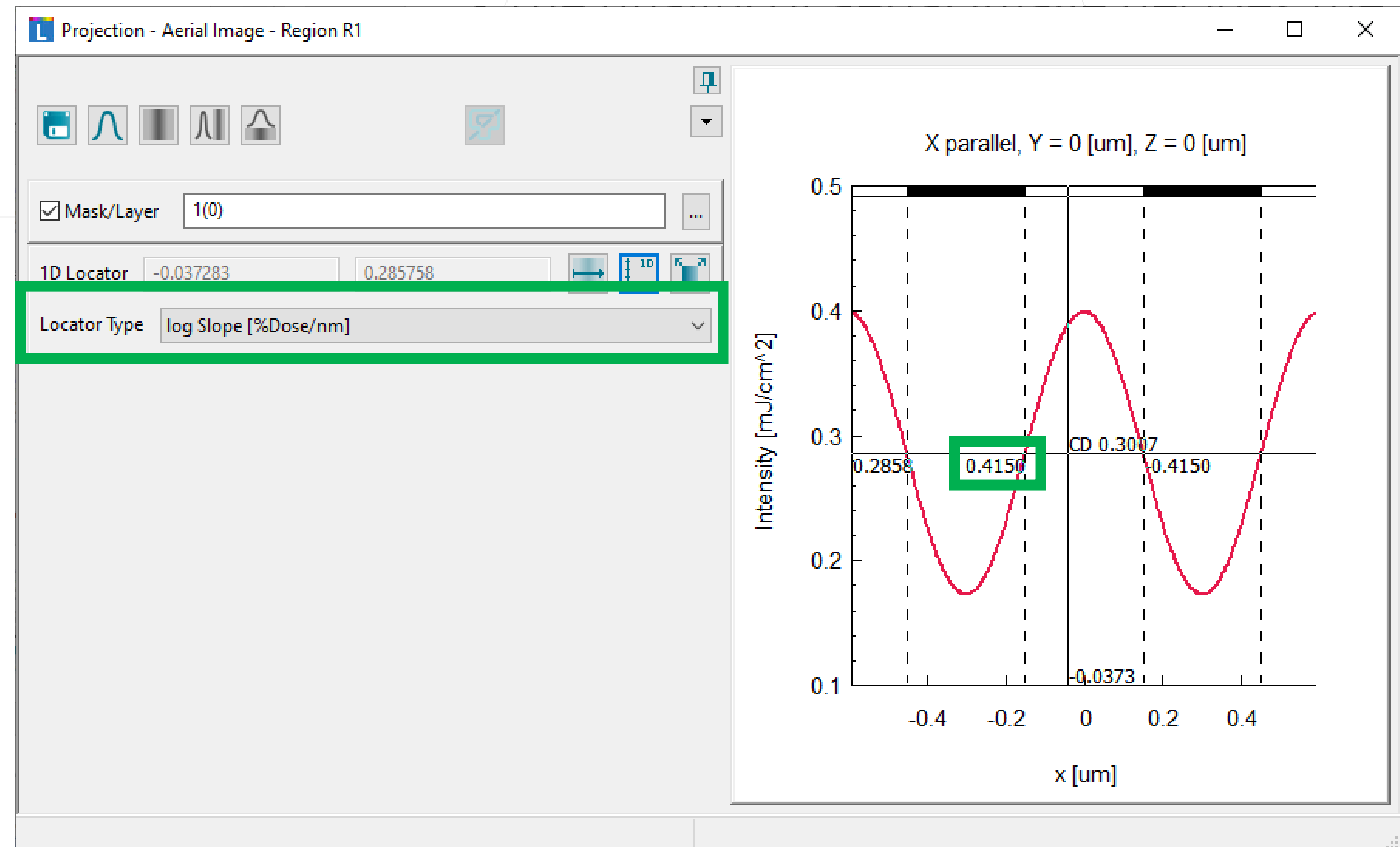
  - image contrast
  - image log slope.

Image log slope = $\dfrac{d(lnI)}{dx}$

Image log slope in 1D intensity image



Attenuated Phase Shift Mask

- To improve the resolution, attenuated phase shift mask (PSM) is one technique.
  - Enhancement of contrast and image log slope improves the resist edge steepness and thus the minimum resolvable CD of the exposure.

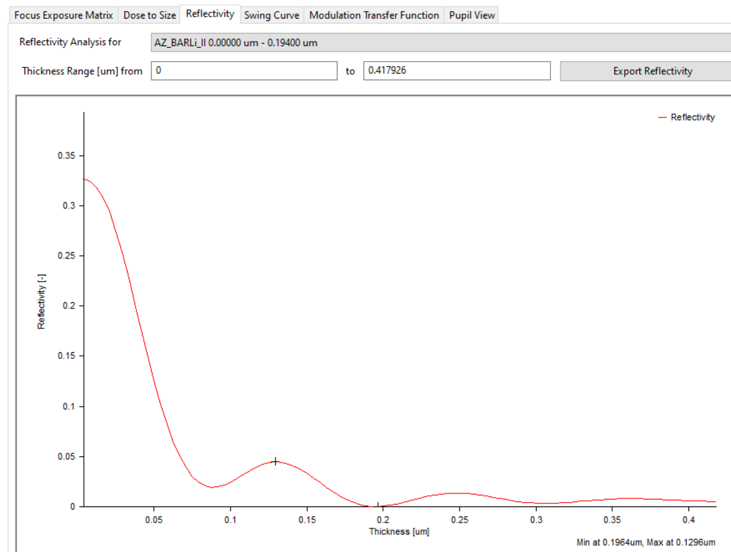
	Image contrast	Image log slope
Normal mask	0.394	0.411
Attenuated PSM	0.535	0.561

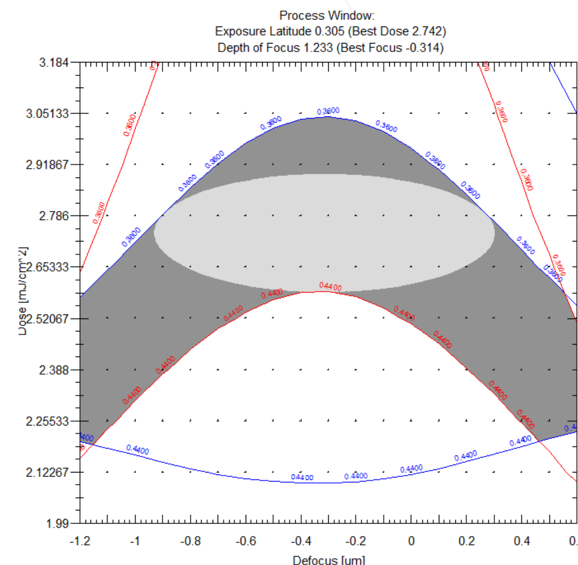
Outline

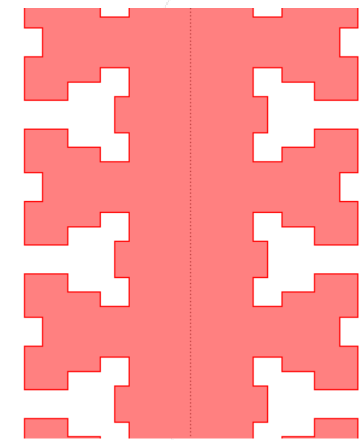
- Projection Exposure
- 3D Exposure Simulation
- Application Cases
  - Stack Optimization
  - Process Window
  - Resolution Enhancement
- Summary

Summary

- Process simulation is a mandatory tool in projection lithography. With a proper model, simulation helps fabrication efficiently. Above all, LAB has been used to
  - design bottom anti-reflection coating to improve process stability
  - Simulate the process window to check the process feasibility
  - design OPC to enhance the exposure resolution and pattern fidelity
  - analyze exposure quality in aerial image







Thank You!

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