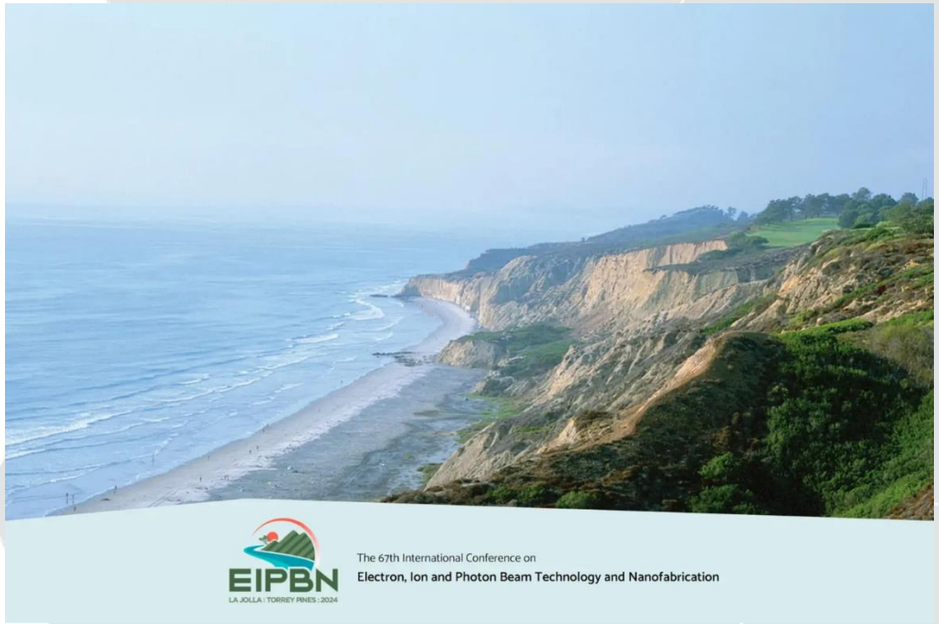
GenISys
Advancing the Standard



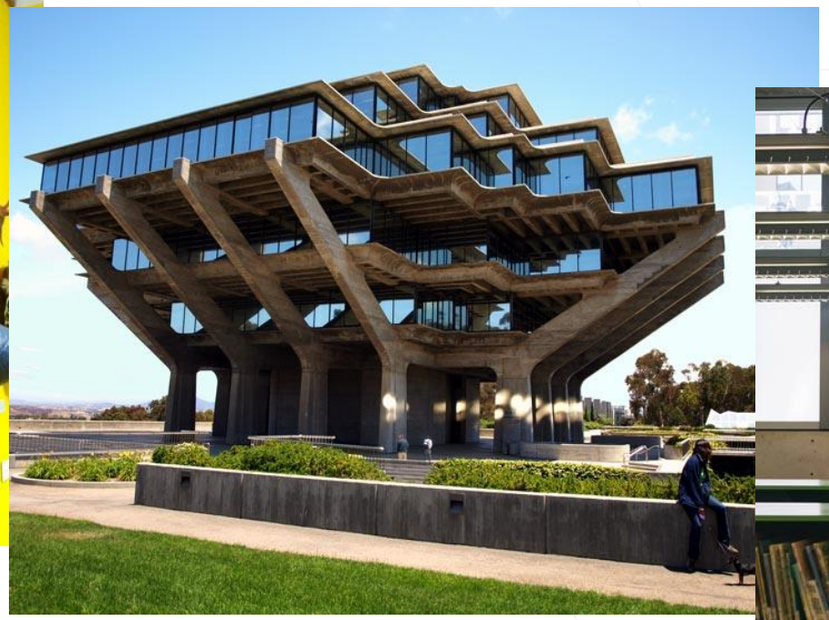
BEAMeeting EIPBN 2024

Technical Workshop & Discussion

BEAMER LAB TRACER MASKER ProSEM InSPEC

Dr. Suess

Legends Gallery



Geisel Library

San Diego Central Library

Be who you are and say what you feel,

because those who mind don’t matter and those who matter don’t mind

Dr. Suess and Computers

If a packet hits a pocket on a socket on a port,
And the bus is interrupted at a very last resort,
And the access of the memory makes your floppy disk abort,
Then the socket packet pocket has an error to report.

If your cursor finds a menu item followed by a dash,
and the double-clicking icon puts your window in the trash;
and your data is corrupted cuz the index doesn't hash,
then your situation's hopeless and your system's gonna crash!

If the label on the cable on the table at your house
Says the network is connected to the button on your mouse,
But your packets want to tunnel to another protocol,
That's repeatedly rejected by the printer down the hall,

And your screen is all distorted by the side effects of gauss,
So your icons in the window are as wavy as a souse;
Then you may as well reboot and go out with a bang,
'Cuz sure as I'm a poet, the sucker's gonna hang!

When the copy of your floppy's getting sloppy in the disk
And the microcode instructions cause unnecessary risk,
Then you'll have to flash the memory
and you'll want to RAM your ROM.
Quickly turn off the computer and be sure to tell your Mom.

https://lynceans.org/all-posts/dr-seuss-explains-why-computers-sometimes-crash/
https://en.wikipedia.org/wiki/A_Grandchild%27s_Guide_to_Using_Grandpa%27s_Computer

About GenISys

GenISys offers software solutions for the optimization of micro- and nano-fabrication processes

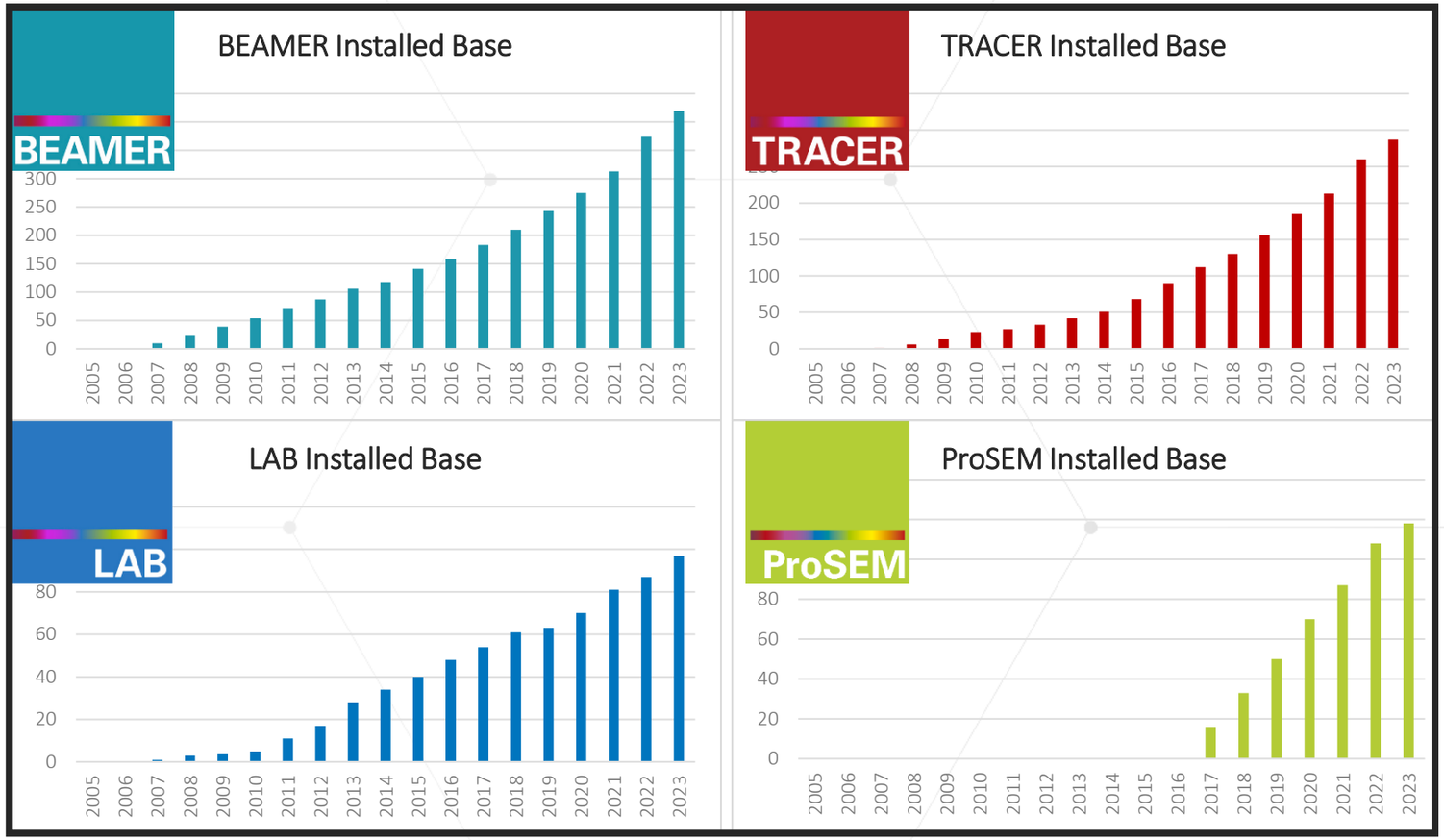
- Founded in 2005 in Munich
  - joined RSBG Group LAB14 in 2018
- Headquarter in Taufkirchen - Munich, Germany
  - Subsidiaries in USA, Japan and Turkey
  - Development locations in Jena, Erlangen & Urla
- Worldwide leader on proximity and process correction for electron and laser lithography processes

GenISys continues to grow while maintaining customer centric spirit!

Products Installed Base 2023

Growing Customer Base (>1000)

- BEAMER and TRACER
  - > 410 BEAMER installation
  - > 280 TRACER installation
- LAB Lithography Simulation
  - > 95 LAB installation
- ProSEM SEM Metrology
  - > 115 ProSEM installation



GenISys – Solution Provider

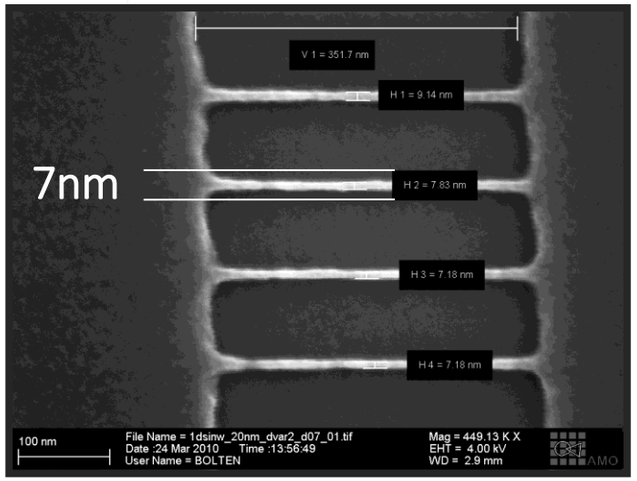
GenISys offers “more than software”:

- Application support including process (~ 10 Application Engineer)
  - Process knowledge from > 200 advanced Nano-Centers
- Active user comunity beyond exposure tool
  - ~ 500 users meet at BEAMeetings worldwide
- Allways at the „spearhead“ of technology with two major releases and frequent patches per year
  - new feature, enhancements and fixes
  - all development is driven by users / equipment partners
  - fast reaction on critical issues (patch in 24 hours)

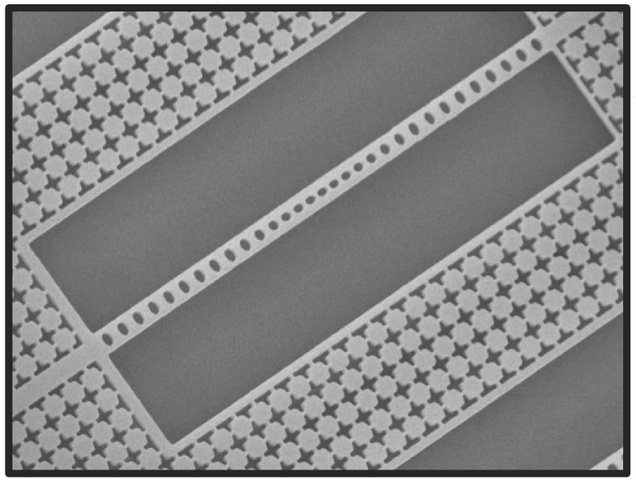
Pushing the limits …

Lithography equipment and processes need optimization to push limits of nano devices:

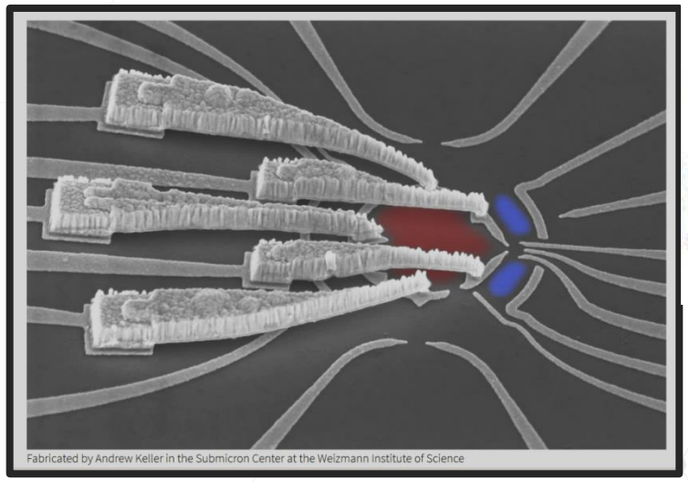
- Proximity and process effects
- Complexity of design and materials



Source: AMO GmbH - Germany



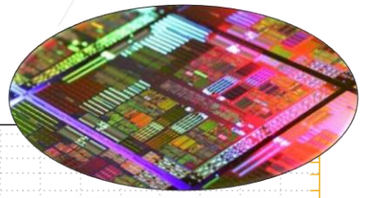
Source: NIST CNST - USA



Source: Weizmann Institute – Israel
Stanford University, USA

Improve Process → BETTER DEVICE

Moore's Law



Number of transistor doubles every two year

Would have failed without MIS

Minimum Feature Size (nm)

10^4 10^3 10^2 10^1 10^0

1970 1975 1980 1985 1990 1995 2000 2005 2010 2015 2020

Year

Transistor Density (mm^2)

10^8 10^6 10^4 10^2

Data from: https://en.wikipedia.org/wiki/Transistor_count

Metrology in Manufacturing

This is how IC manufacturing patterns…

Images vendor webpages

This is how IC manufacturing measures…

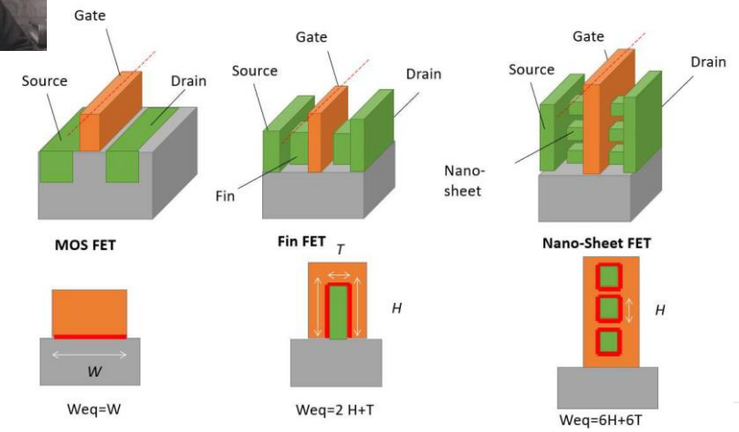
Image AMAT webpage

- Consistent and reliable measurements are critical for IC manufacturing
  - Fully automated, very fast, consistent using reliable algorithm
  - CDSEMs are expensive and inflexible – not affordable for most nanofabrication facilities

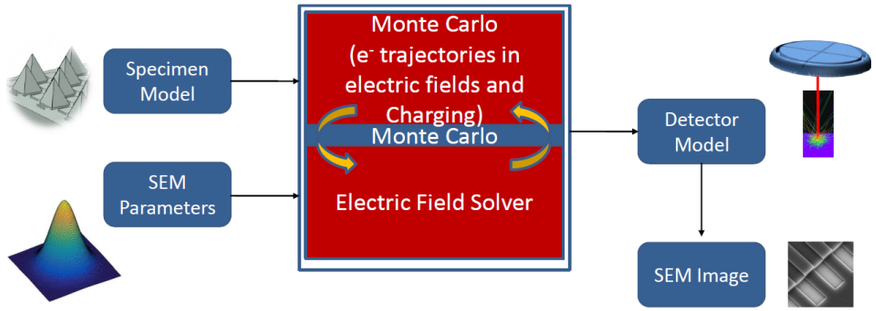
Metrology & Inspection (MIS)

- "If you cannot measure it – you cannot improve it"
  - Lord Kelvin

- Inspection is becoming bottleneck for IC production
  - New structures need to be developed based on inspectability
  - Key enabler: computational MIS, SEM Simulation



- GenISys vSEM technology is a serious contender
  - Scattering kernels market validated
  - Charging solved in principal

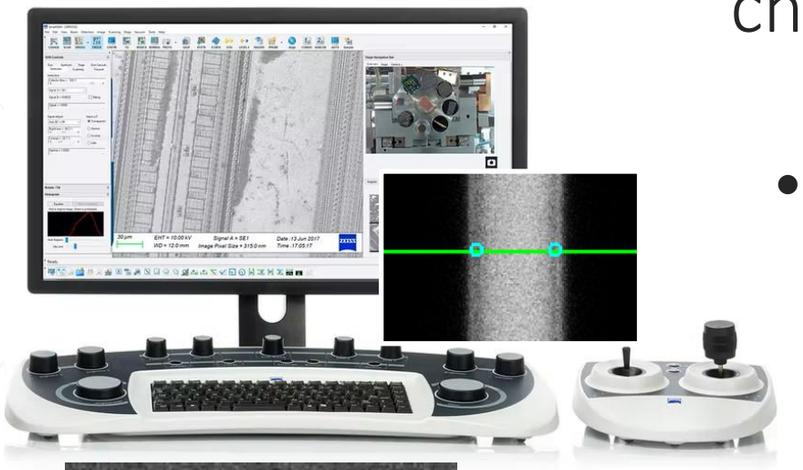


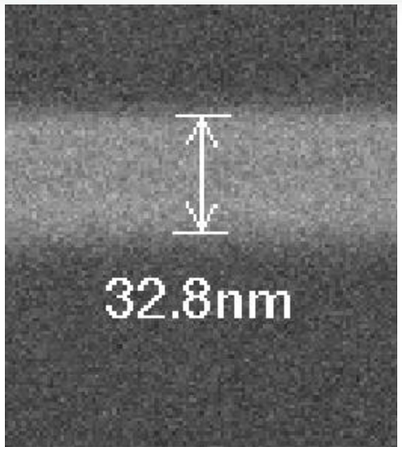
- GenISys continues to invest large resources into MIS
  - ProSEM, SEM Automation
  - Die-to-Database inspection platform
  - vSEM SEM simulation

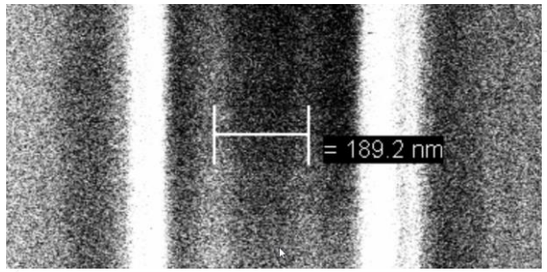
The Metrology Challenge in Nanofabrication

This is how you create nano patterns…

This is how you measure nano patterns..?







- Consistent and reliable SEM measurements are critical for process characterization
  - Hand-drawn cursors are subjective, tedious, time-consuming, inconsistent

Images vendor webpages

GenISys
Advancing the Standard

Upgrade SEM to a CD-SEM by Software

This is how you measure nano patterns..?

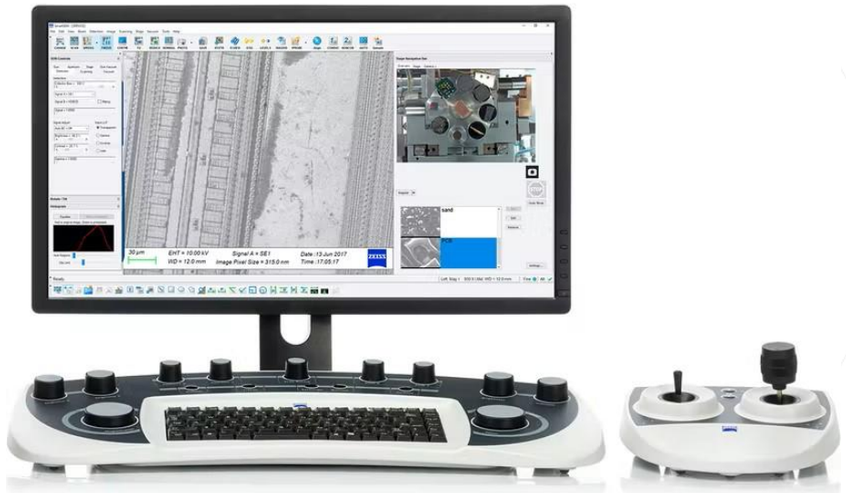
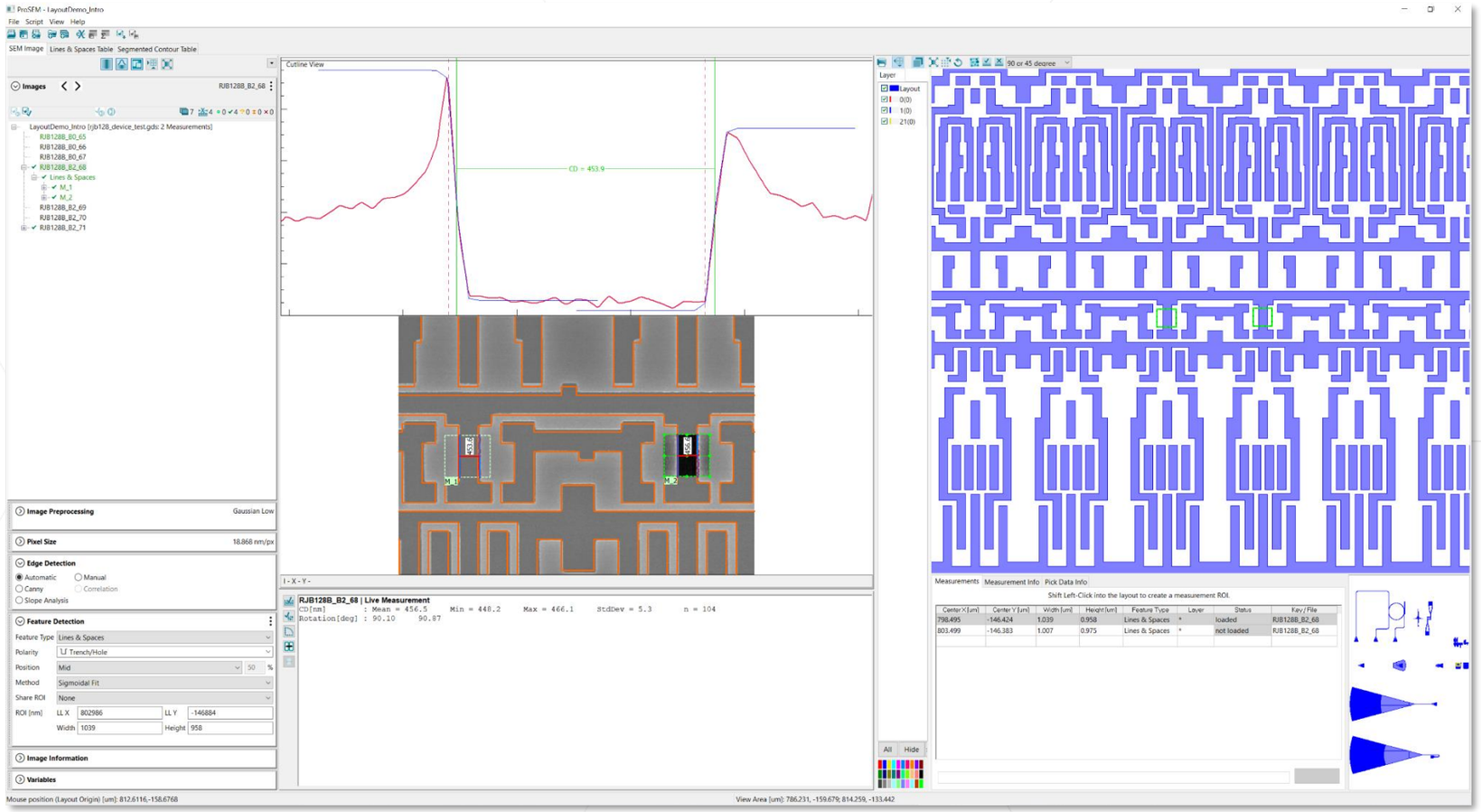


Image ZEISS webpage



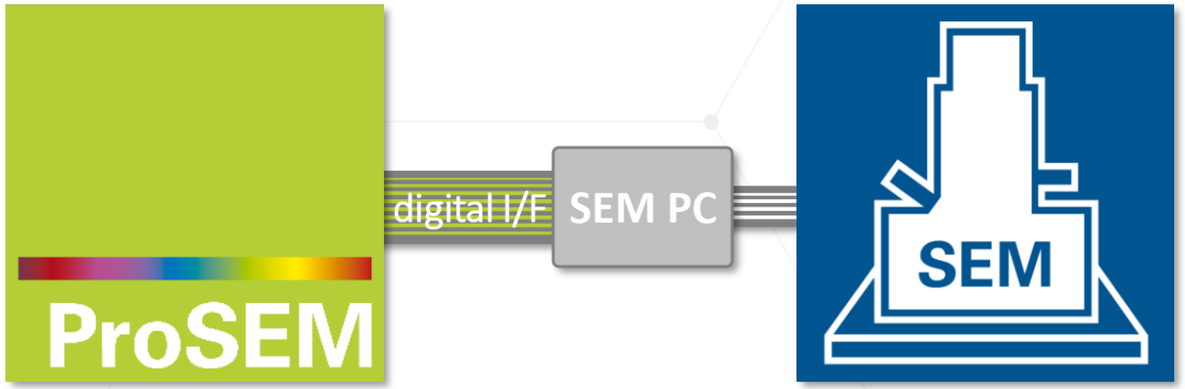
Algorithm-based Easy Metrology

Advanced Pattern & Batch Processing

Aligned CAD Layout Integration

Digital Interface SEM Automation

Make „More“ out of your SEM



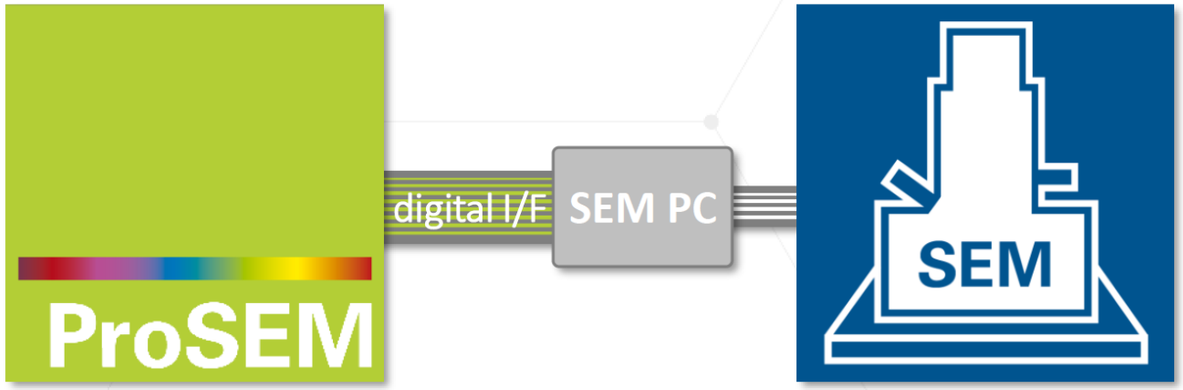
Remote control of SEM via digital PC interface

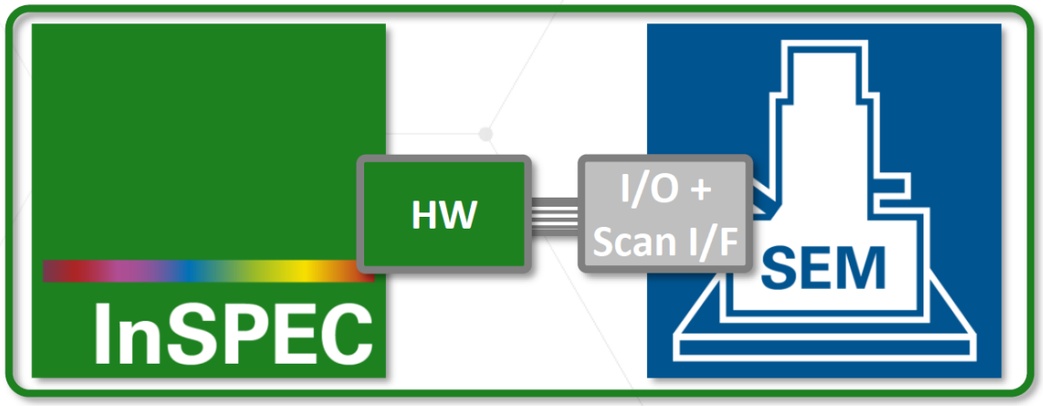
Easy to get SEM images and metrology results

Automated metrology

- Layout based metrology definition (no scripting!)
- Drive SEM stage and acquire image
- Image loading and alignment
- Apply pre-defined measurement automatically

Next level …





Remote control of SEM via digital PC interface

Easy to get SEM images and metrology results

Direct SEM control with hardware integration

Comprehensive full layout-based workflow

Integrated scanning, automation and analysis

E-Beam Process Calibration

TRACER enables to identify the optimal process point in a simple experiment

- prooven for multiple substrates (Si, SiO2, GaAs, InP, …)
- prooven for typical direct write resists (PMMA, ZEP, HSQ, …)
- demonstrated for CAR resists (both positive and negative tone)

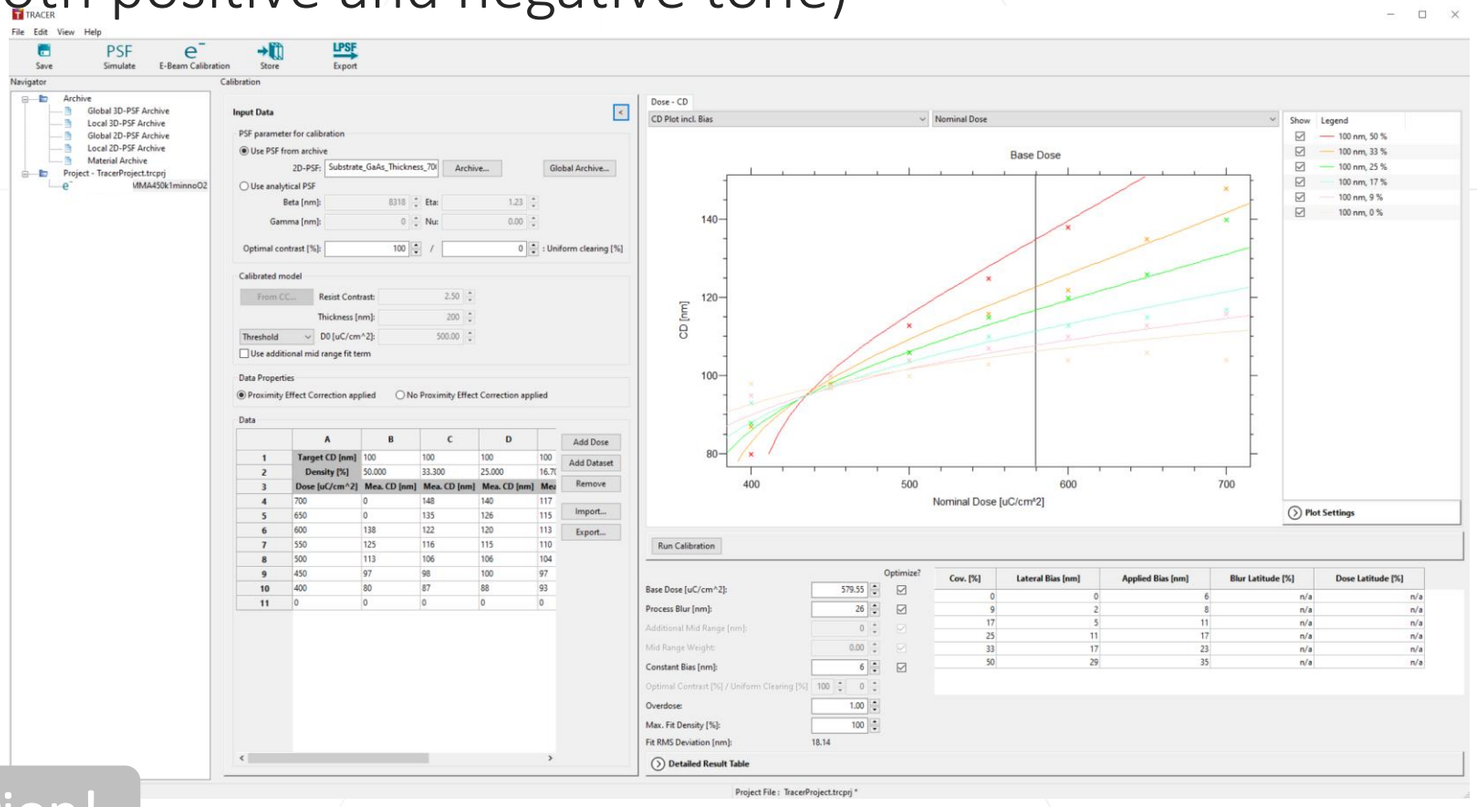
Universal approach for process optimization of chemically amplified photoresists in electron beam lithography

Markus Greul,[a,*] Astrit Shoshi,[a] Jan Klikovits,[b] Stephan Martens,[a] Holger Sailer,[a] Olga Barahona[a], Benyamin Shnirman,[a] Leon Starz,[a] Jan Hofmann,[b] Patrick Wintrich[a]
[a]Institut für Mikroelektronik Stuttgart SdbR, Allmandring 30a, 70569 Stuttgart, Germany
[b]GenISys GmbH, Eschenstraße 66, 82024 Taufkirchen (Munich), Germany

Abstract. A critical factor in the fabrication of complex nano- and microstructures with high quality and reproducibility is the determination of a suitable working point. This applies particularly to lithography, which is the basis for transferring the desired patterns onto the substrate. For this reason, the following paper presents a generic process optimization methodology that has been successfully applied to four chemically amplified positive and negative tone electron beam lithography photoresists with different sensitivities. The method is iterative and designed for best possible results with a minimum use of resources. This is accomplished by identifying the critical key factors in photoresist processing using contrast curves and determining their impact. Starting with the most influential bake parameter, the maximum effect is achieved. The method used is similar to the *Bossung*-plot procedure and aims for a maximum process window. After the bake parameters, the fundamentals of development kinetics are discussed and a method for determining an appropriate development time is presented. A mask making approach is then used to investigate the ideal exposure conditions. This includes the determination of an appropriate base dose in conjunction with proximity effect correction and sizing. The evaluation of this method is demonstrated by critical dimension linearity plots and scanning electron microscope cross sectional analysis of resist profiles. The results presented impressively demonstrate the universality of the optimization approach.

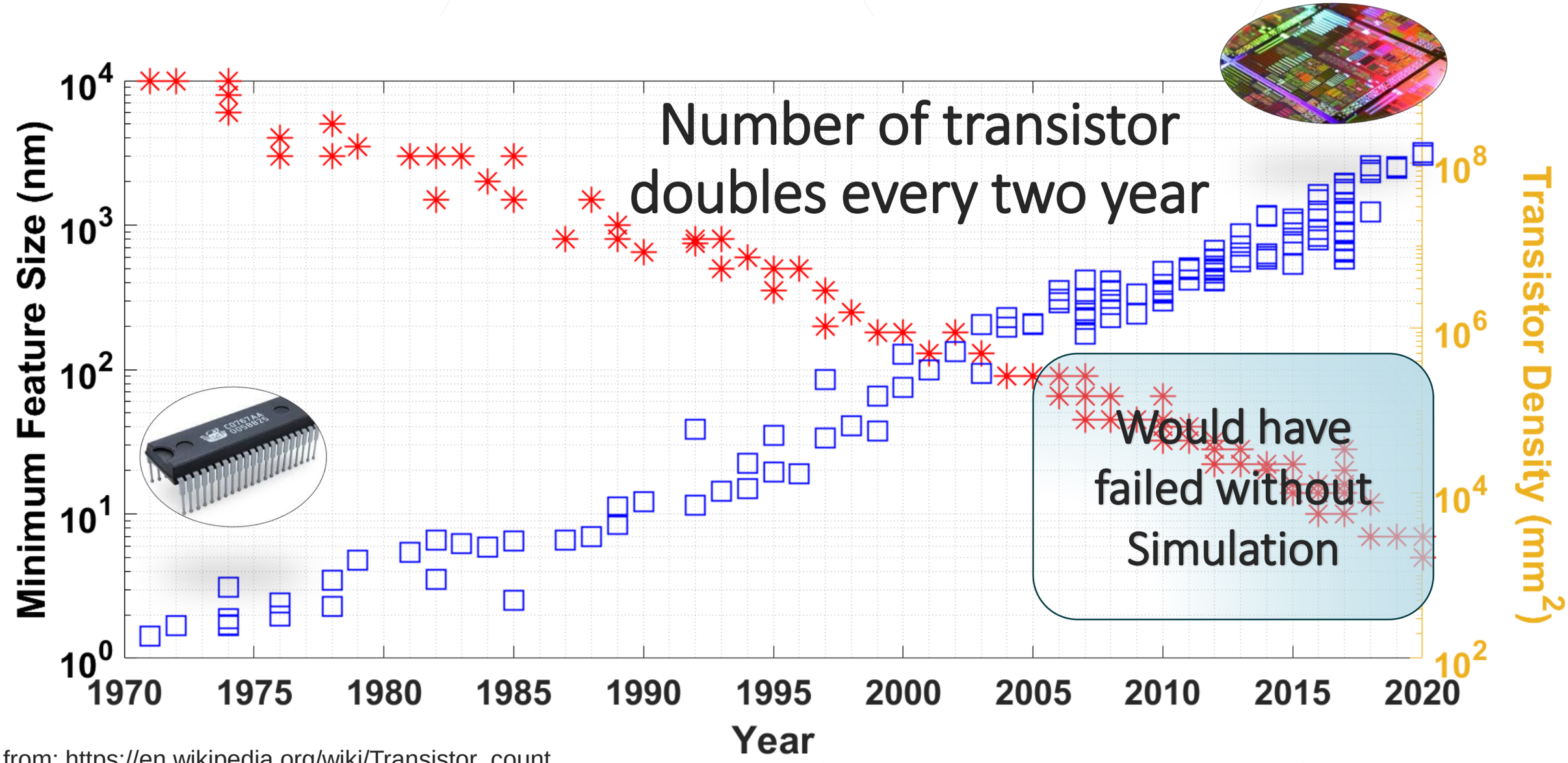
Keywords: electron beam lithography, photoresist process optimization, nano- and micro-patterning, photoresist bake, development, proximity effect correction (PEC), point spread function (PSF).

*Markus Greul, E-mail: greul@ims-chips.de



"Peace of Cake" with ProSEM Automation!

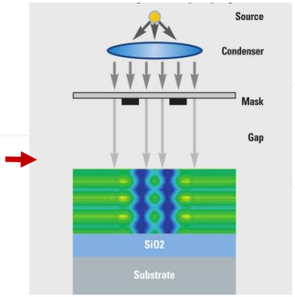
Moore's Law



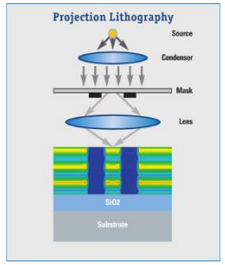
Data from: https://en.wikipedia.org/wiki/Transistor_count

Simulation Flow

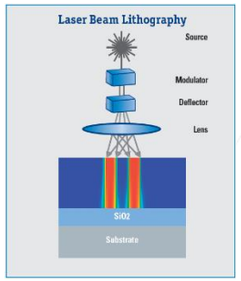
Mask Layout



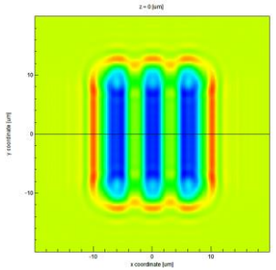
Proximity

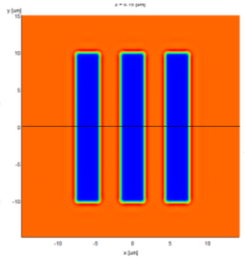


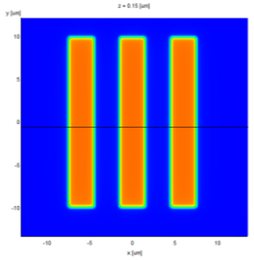
Projection

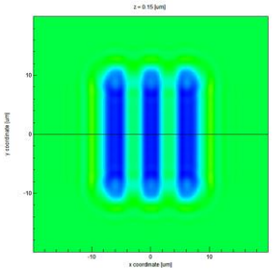


Laser

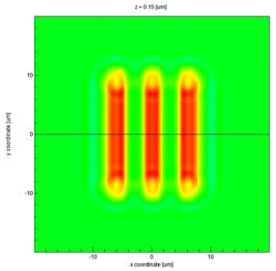




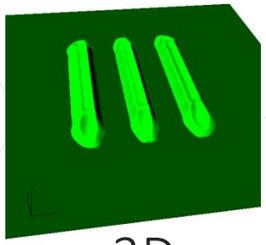




Bulk



Concentration



3D Resist

Aerial

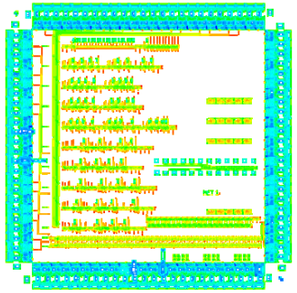
Bulk Intensity

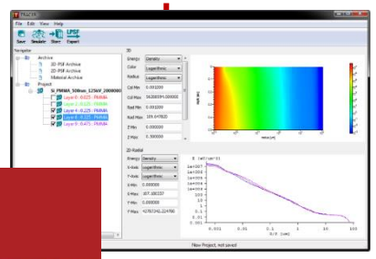
Concentration

3D Resist

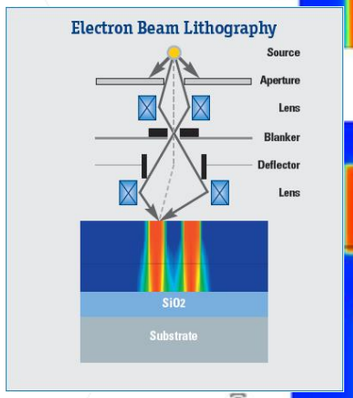
3D e-Beam Lithography Simulation

Layout

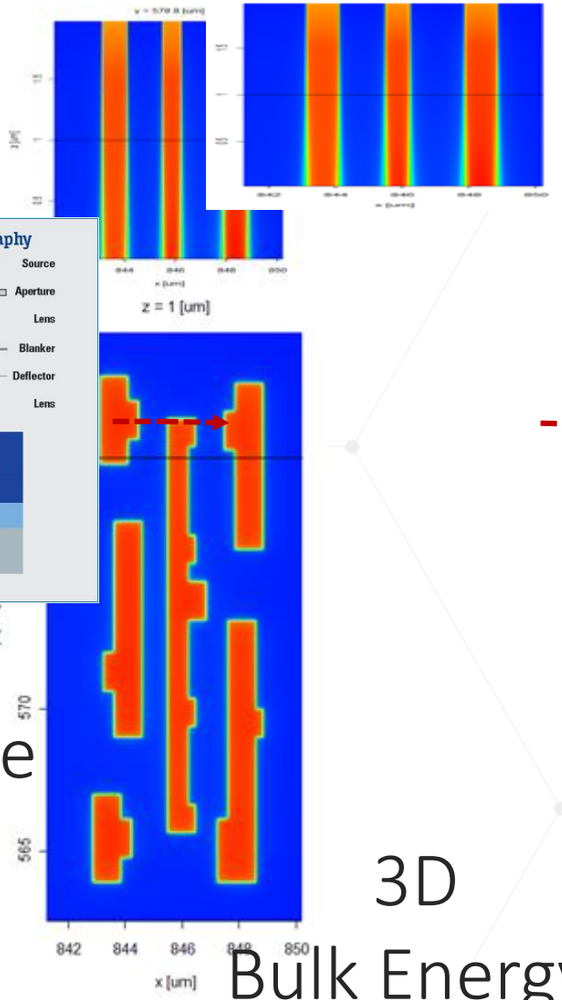




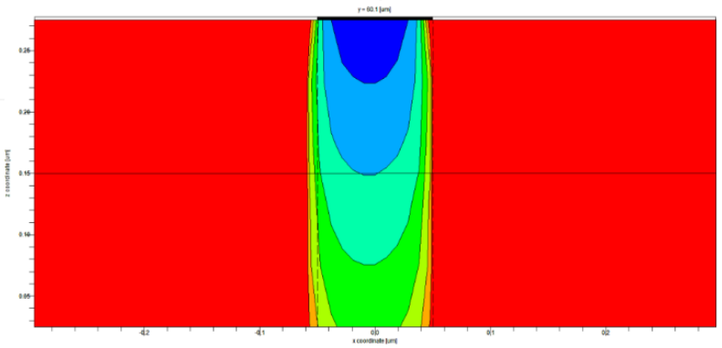
3D PSF

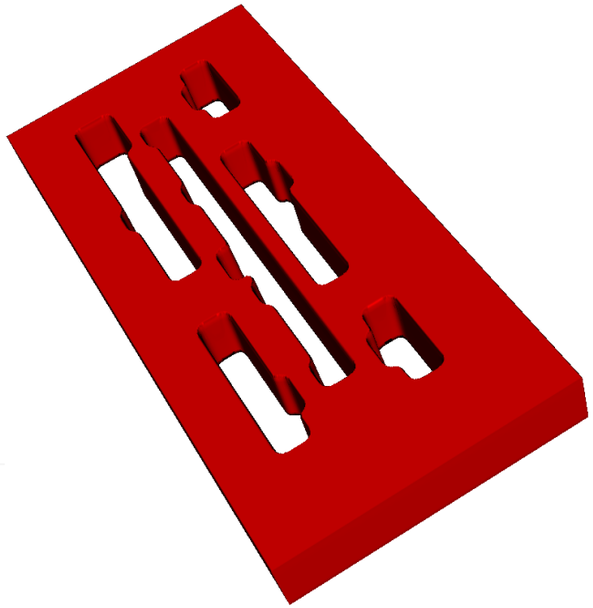


E-Beam Exposure



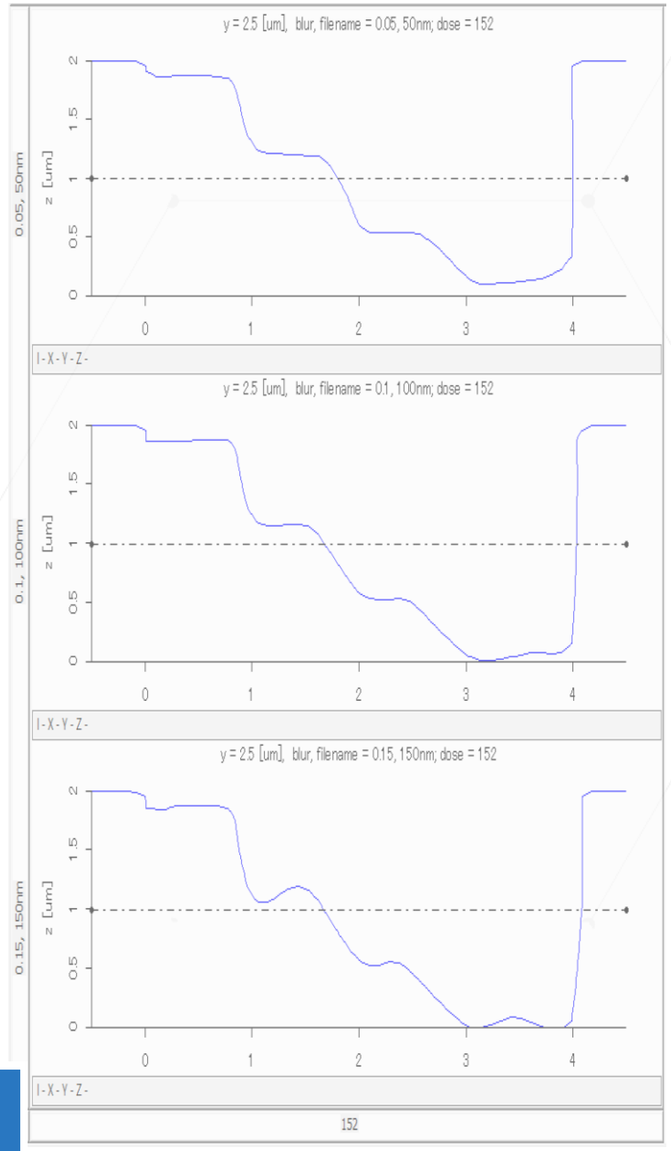
3D Bulk Energy





3D Resist Development

E-Beam 3DPEC & LAB (BushClover)



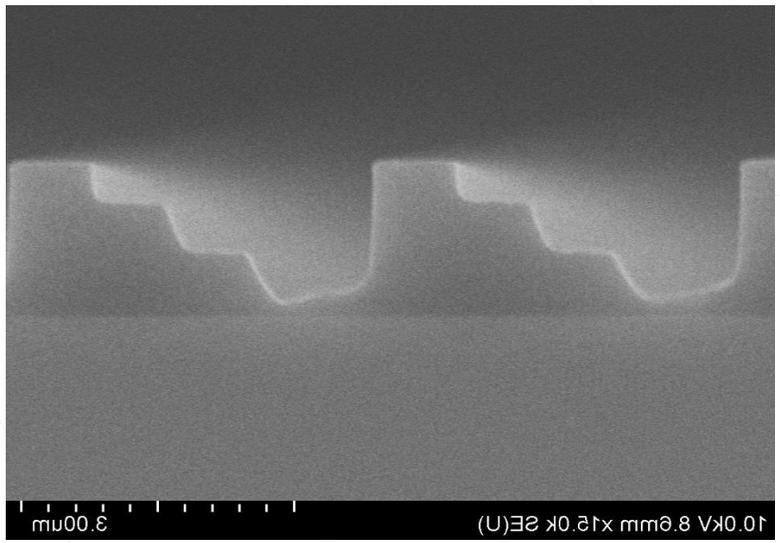
50nm

Blur 100nm

150nm

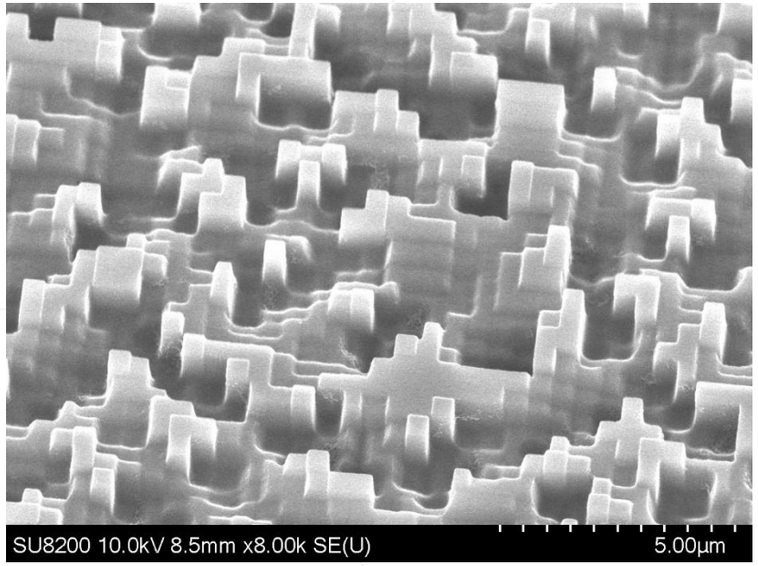
LAB

Dose 152 uC/cm2



E-Beam 3D, data prep. by BEAMER.
→ Compared with LAB simulation.

BEAMER

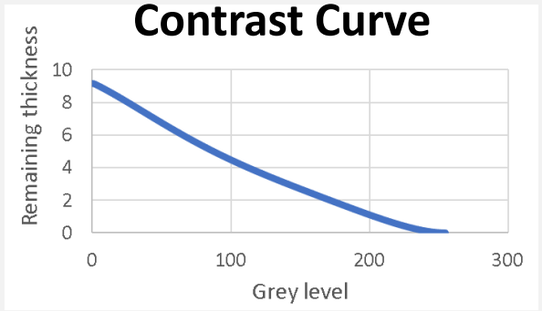


Stable results are obtained by BushClover (Mr. Nizeki)

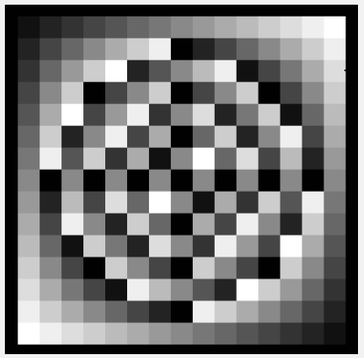
Simulation of Laser Exposure Process

Input

Contrast Curve

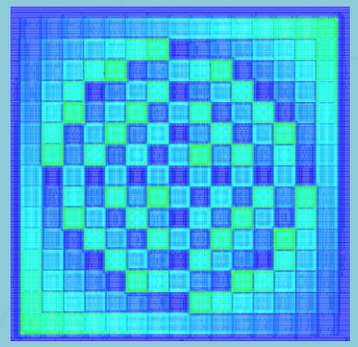


Layout



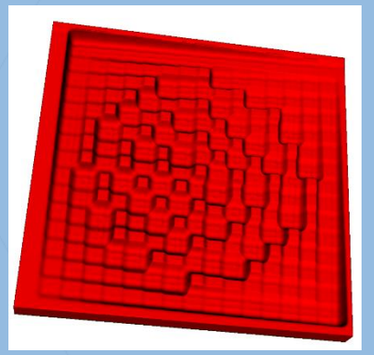
BEAMER

Calculated energy distribution

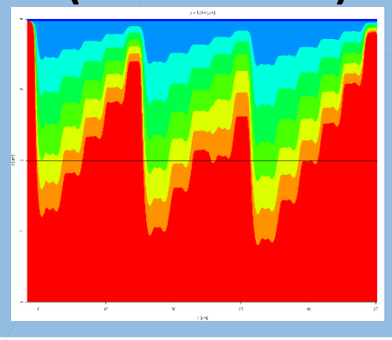


LAB

Simulated 3D profil (after development)



Development process (Crosssection)

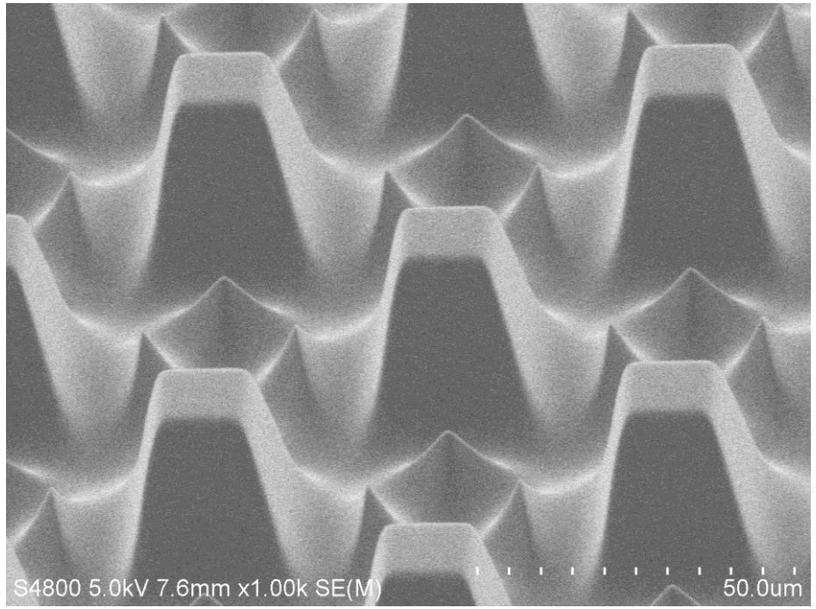


Result

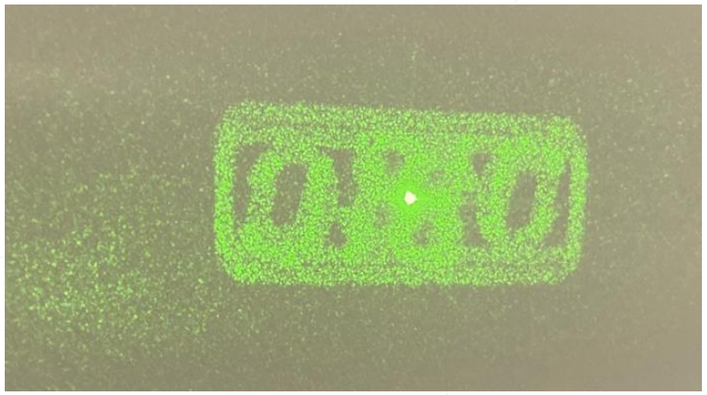
Developed sample

Laser 3DPEC

Resist : PMER P-HA 300
pre-bake: 90 °C, 6min
By BushClover

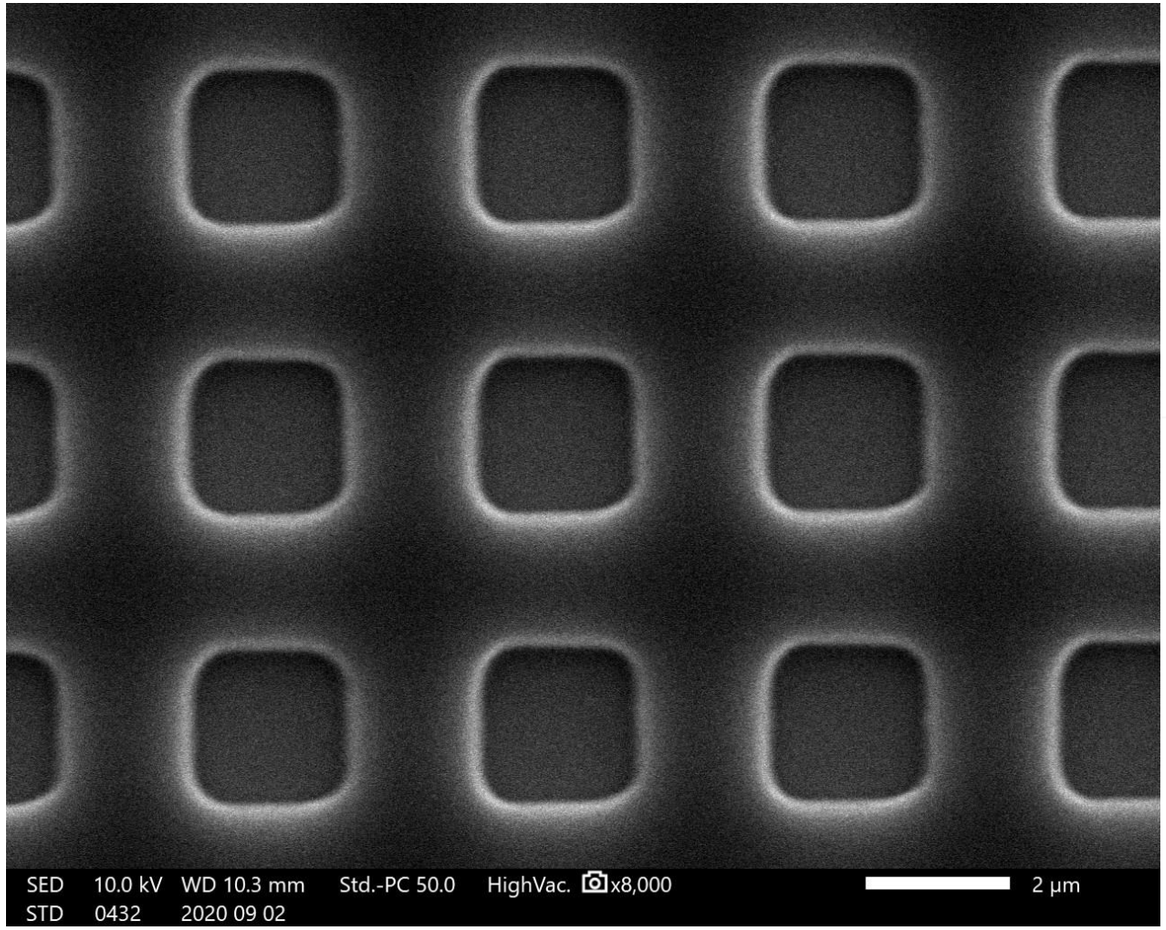


1um pixel size DOE for green laser optics.
DOE steps: ca. 200nm

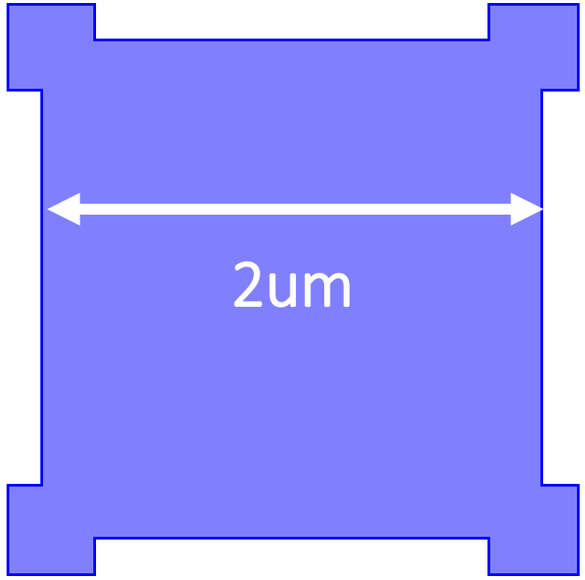


2um Square Dots

without correction



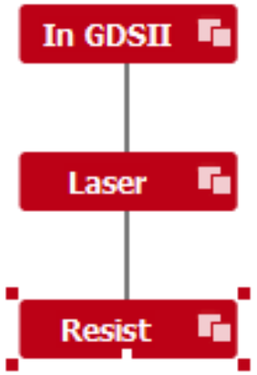
Optimize serif size & overlap influences by simulation

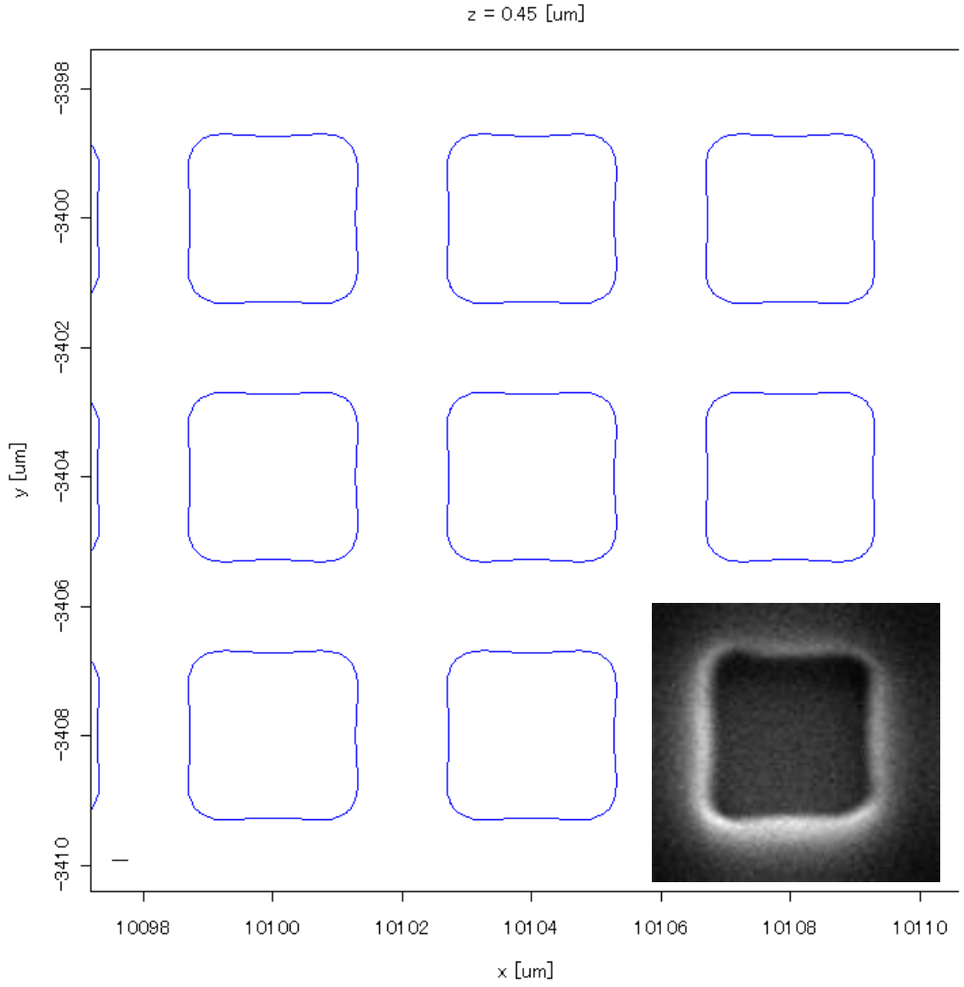


Rule-OPC

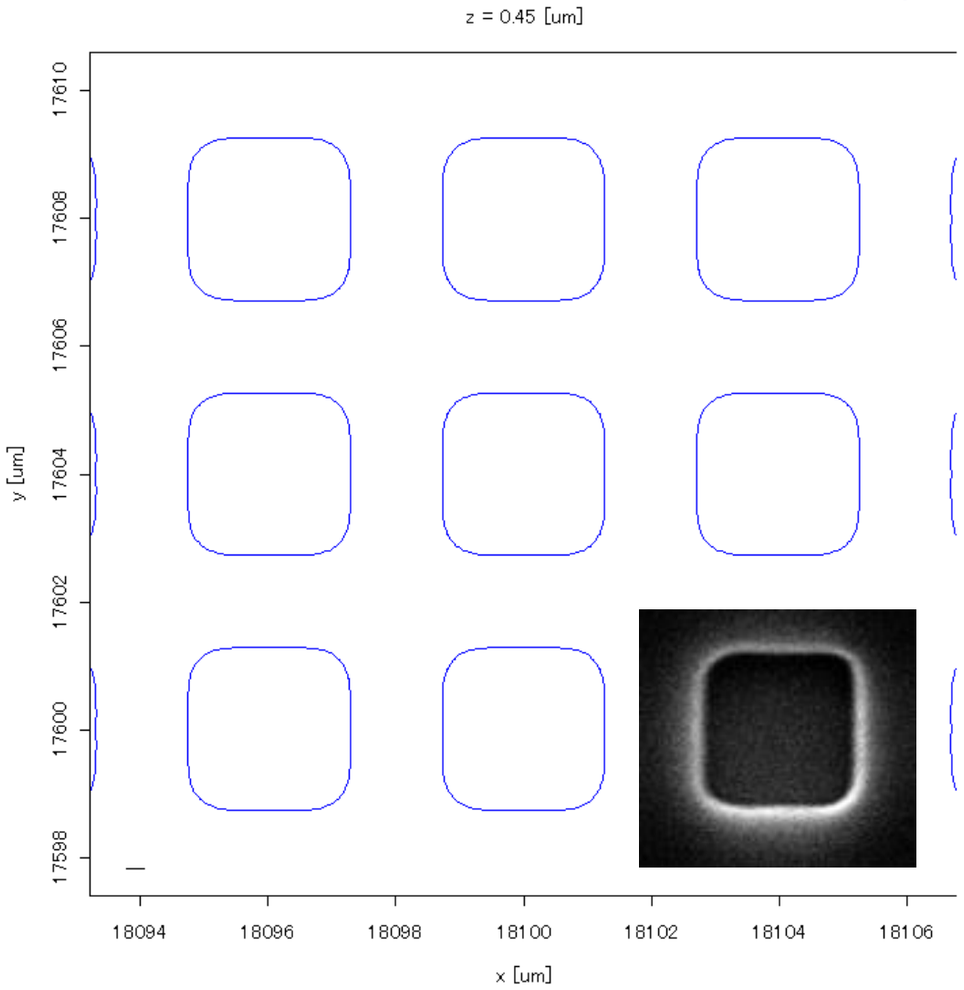
LAB Simulation : 2um Square Dots

350nm Serif with 60% overlap



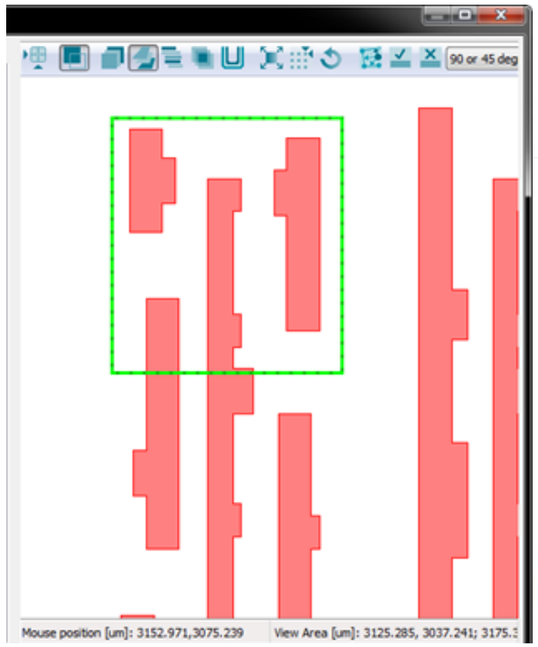


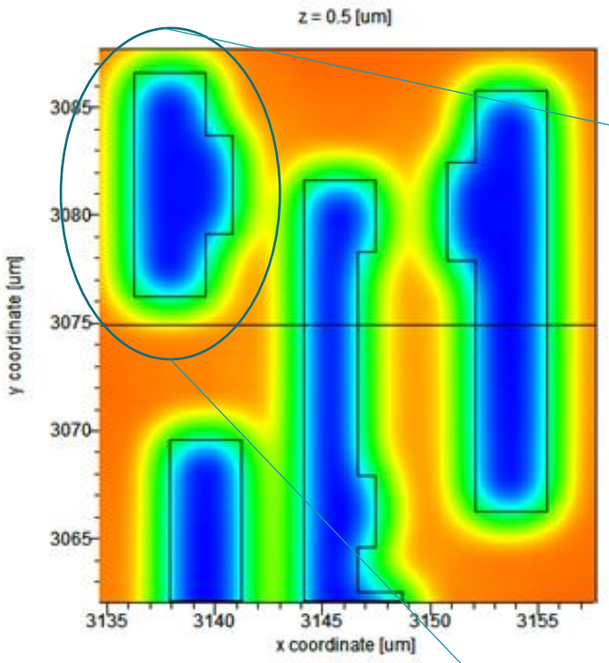
200nm Serif with 70% overlap

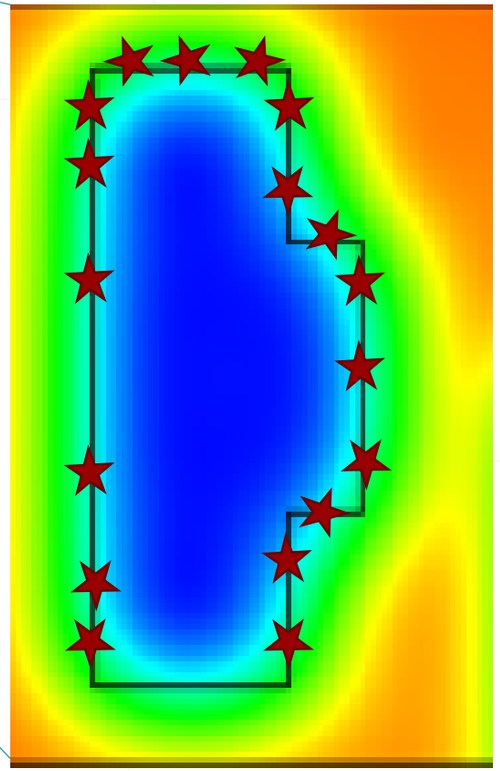


Simulation is able to predict proper serif size in advance

Model-OPC for Projection (Stepper)



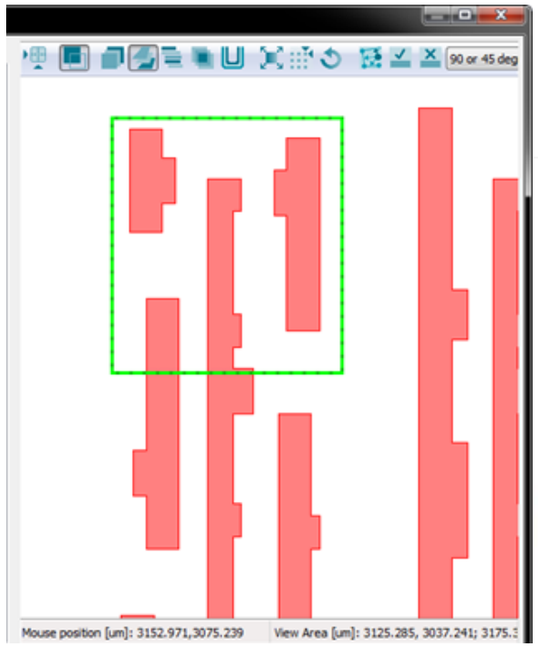


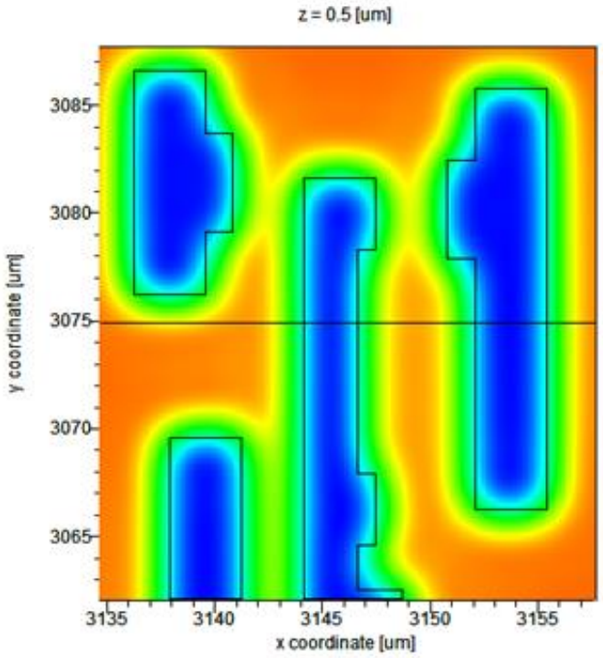


Fully automated correction:

- Iterative process
- The exposure is modelled at layout edges (fast simulation)
- Placing of evaluation points at layout edge
- Compare intensity level
  - at taget: no action
  - Below or above target: move edges

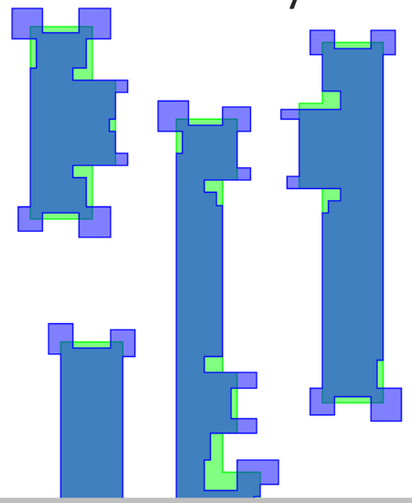
Model-OPC for Projection (Stepper)





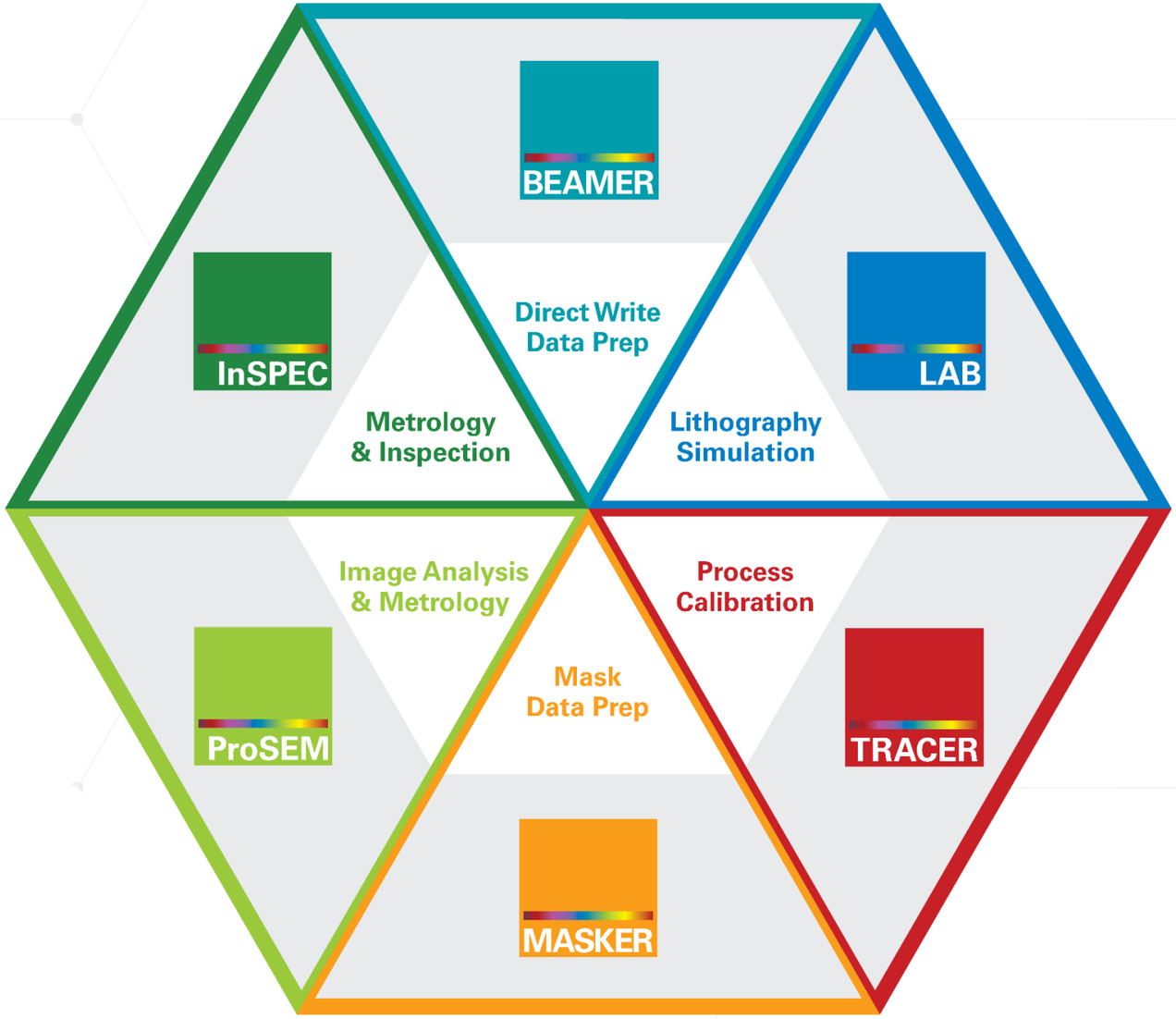
Fully automated correction:

- Iterative process
- The exposure is modelled at layout edges (fast simulation), compared to target
- the layout is modified (shape correction) to compensate for mismatch
- Full layout import



GenISys is offering Full-Chip OPC for special and mature application!

Come by our Booth…



Agenda

BEAMeeting E-Beam & Laser Workshop Technical Workshop & Discussion		
Tentative Agenda		
	LIGHT BREAKFAST	8:30 am
Ulrich Hofmann GenISys	**Welcome & Introduction GenISys Update**	9:00 am
Nezih Unal GenISys	**Laser Simulation and Process Calibration**	9:20 am
Bethany Niedzielski Huffman MIT Lincoln Labs	**Quantum Computing and Electron Beam Lithography**	9:40 am
Marvin Zai GenISys	**Building Bridges in Beamer with 3D Edge PEC**	10:00 am
Bernadeta Srijanto Oak Ridge National Laboratory	**Maximizing process efficiency with dual current exposure strategy**	10:20 am
	Coffee Break	10:30 am
Sven Bauerdick GenISys	**Unveiling the NEW InSPEC**	10:50 am
Leonidas E. Ocola IBM	**"*So you think you know eta in PEC …*"**	11:10 am
Dengyang Lu University of Pennsylvania	**Image processing and Data Preparation for Structural Color Generation**	11:30 am
Roberto Panepucci Cornell NanoScale Facility	**Distortion Correction and Application**	11:50 am
	Lunch	12:10 pm
Chad Eichfeld Penn State University	**Automated SEM Metrology Use Cases for InSPEC**	1:00 pm
Benedikt Stender Heidelberg Instruments	**MPO 100: The Future of 3D Nano- and Micro-Lithography**	1:20 pm
Kaustubh Vyas GenISys	**Radial PEC, Powerful Filter & the new Fields module**	1:40 pm
	Coffee Break	2:00 pm
Sven Bauerdick GenISys	**ProSEM vs. InSPEC: the "best" metrology solution**	2:20 pm
Nezih Unal GenISys	**What's New in BEAMER Roadmap Discussion**	2:30 pm
	FINAL Closing	3:00 pm

Thank You!

support@genisys-gmbh.com

Headquarters
GenISys GmbH
Eschenstr. 66
D-82024 Taufkirchen (Munich)
GERMANY
+49 (0)89 954 5364 0
+49 (0)89 954 5364 99
info@genisys-gmbh.com

USA Office
GenISys Inc.
P.O. Box 410956
San Francisco, CA
94141-0956
USA
+1 (408) 353 3951
usa@genisys-gmbh.com

Japan / Asia Pacific Office
GenISys K.K.
German Industry Park
1-18-2 Hakusan Midori-ku
Yokohama 226-0006
JAPAN
+81 (45) 530 3306
+81 (45) 532 6933
apsales@genisys-gmbh.com